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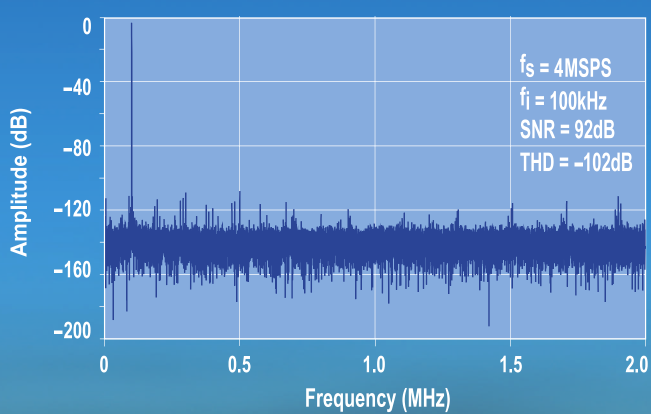

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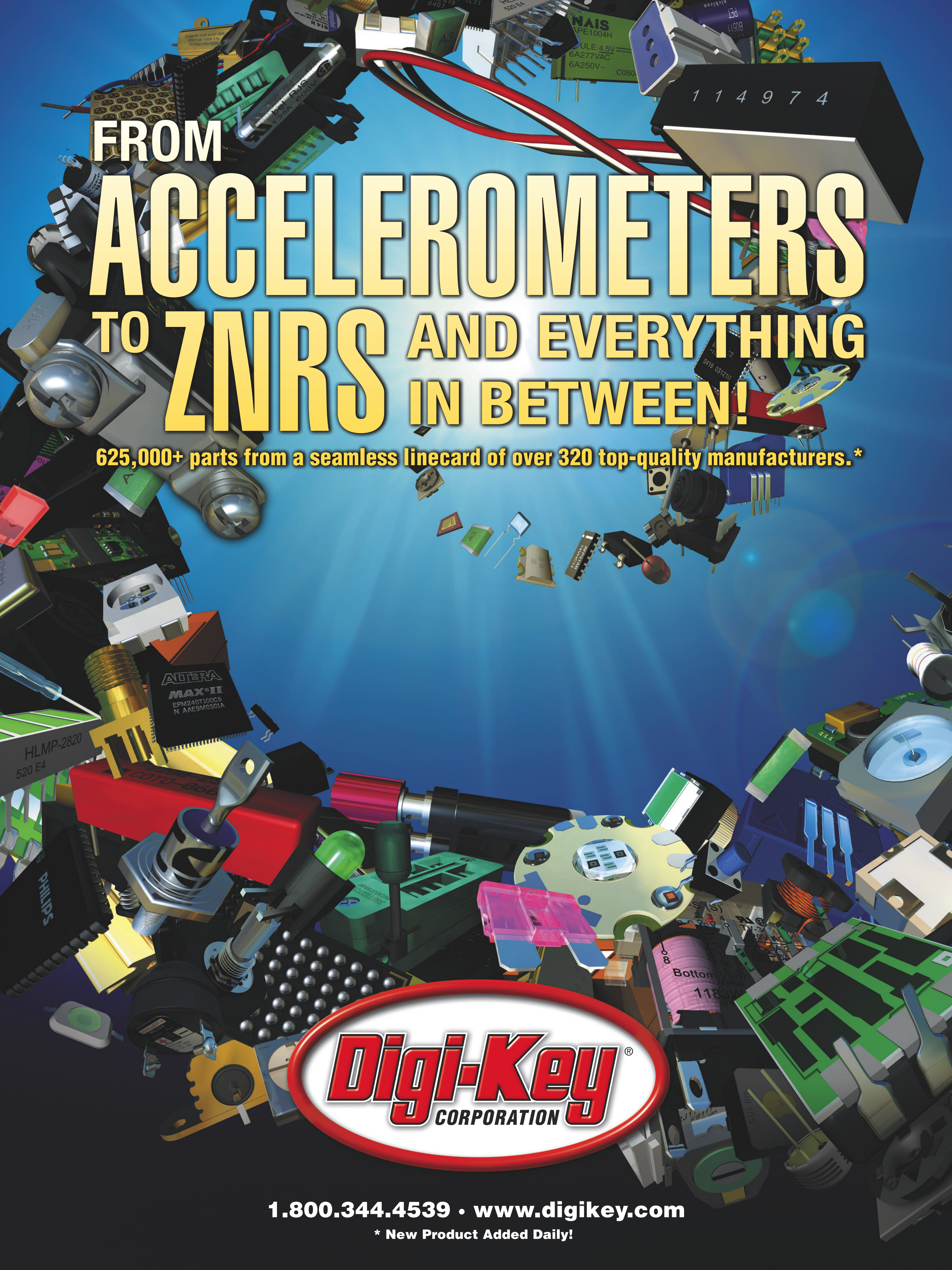
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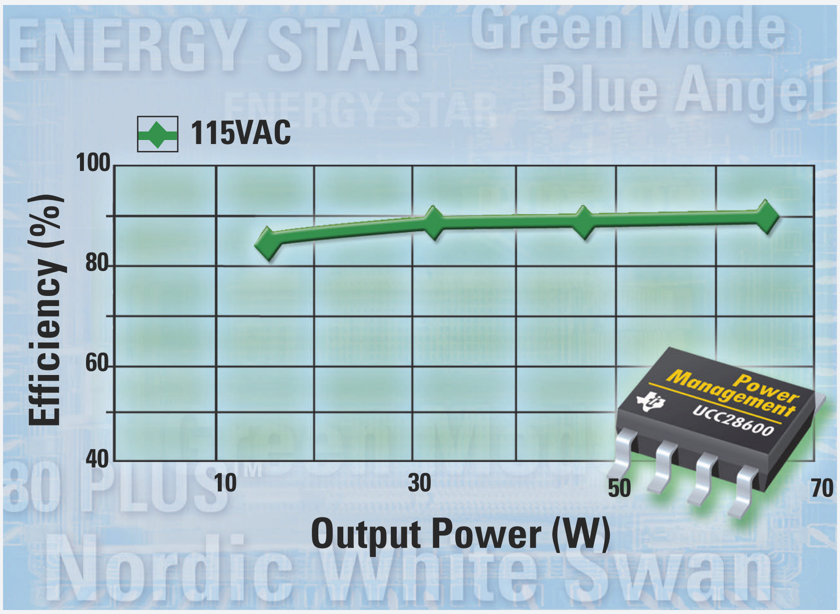

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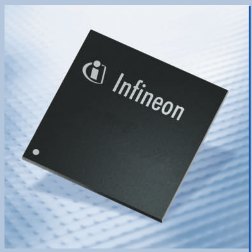

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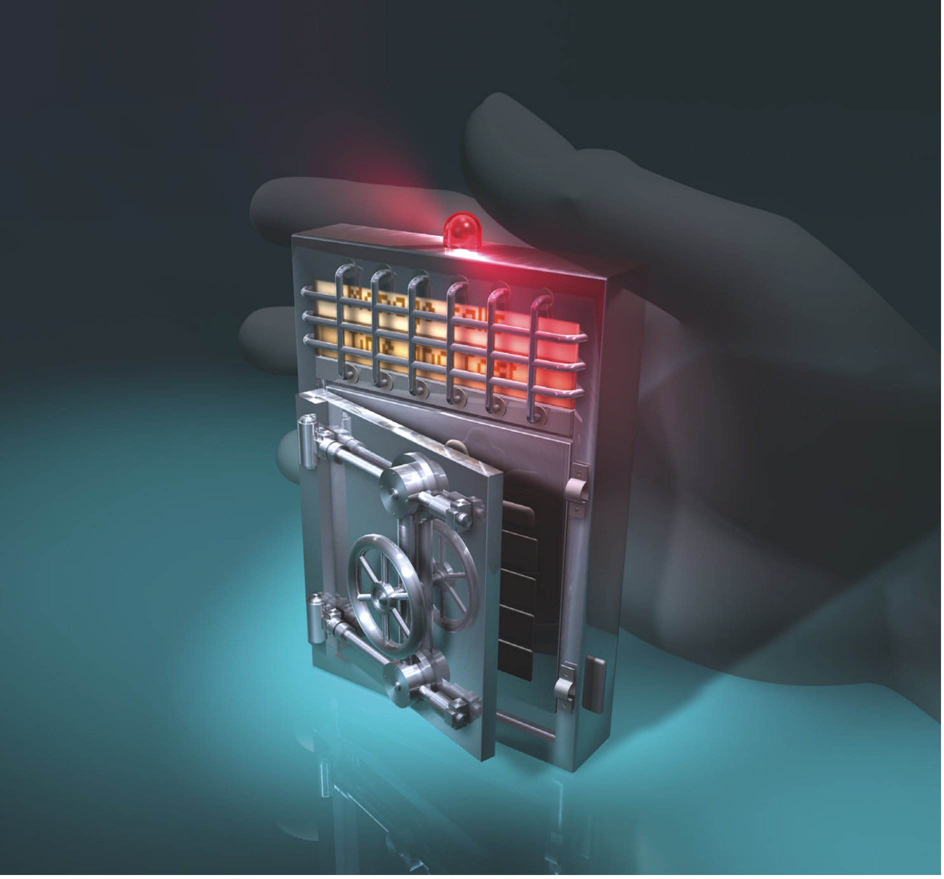

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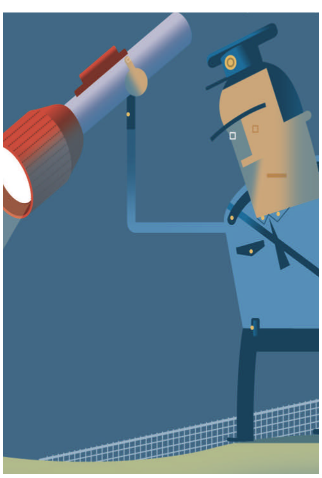

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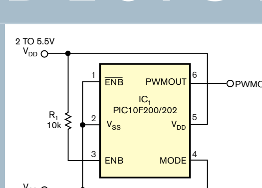

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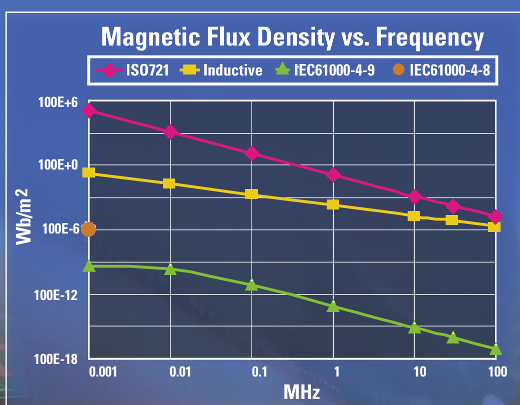

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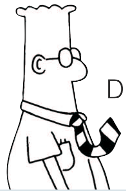

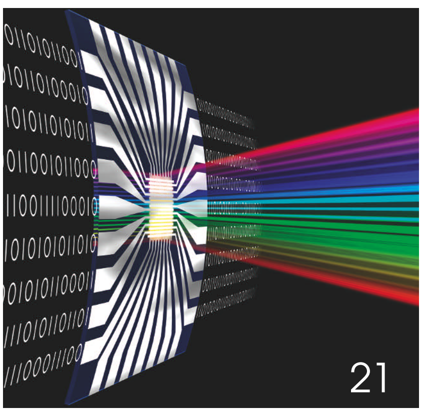

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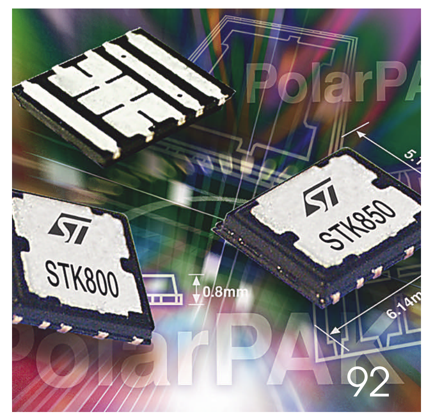

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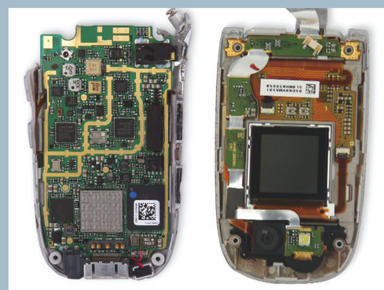

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BY MAURY WRIGHT, EDITOR IN CHIEF

Contextually correct search: a timesaver for engineers

If you've recently visited our Web site, www.edn.com, you may have noticed a new search feature, Zibb, in a rectangular, blue box near the top of the page. Our parent company, Reed Business Information, developed Zibb, a search engine that aims to provide contextually correct searches and promises to save users time by returning only relevant search results.

We know from our ongoing research efforts that you constantly use search engines in your daily work. And, like the world at large, engineers primarily use Google, although some also use other options, such as Yahoo and Ask. In fact, you have told us that you will use Google to find information on a vendor's Web site, because Google can often get you to the correct place faster than the vendor's own site search. And we know that many of you use Google to find articles on our site and come to visit following a Google link.

EDN and Reed Business appreciate Google and the traffic that it brings us. In fact, our company has partnered with Google on several initiatives. But we also know that Google isn't perfect. There are still many words that we use in the tech industry that have far different meanings when you use them in broader society. As good as Google is, it often delivers more meaningless links than relevant ones on tech-centric searches. We believed that we could develop an industry-centric search engine to serve vertical communities, such as electronics. The result is Zibb, and a couple of months ago, *EDN* became the first site in the Reed universe to roll out the engine.

We rely on the Zibb technology both to greatly improve our site search and to provide contextually correct, broader industry searches. The Zibb box that appears on every *EDN* Web page is simply a site search. We present it that way because we have many regular visitors who have long used our site-search facility on each page. Having Zibb on each page provides the exact same user interface that the old site search offered. But try it, and I think you will agree that it performs far better than the old site search.

If you click on the Zibb logo to the left of the search box (or go to www.edn.com/zibb), you will reach a search-landing page that offers additional capabilities. You will reach a similar page whenever you do a site search, as well. The dedicated Zibb search page offers tabs above the search box that allow you to expand your search.

The default tab is the *EDN* site search. To the right of that tab is one labeled "news." The news tab produces results strictly from electronics-industry trade publications, including our competitors. The next two tabs, products and companies, are works in progress. Note that Zibb is officially still in beta status. But the products and companies tabs will ultimately tie to another Reed Business property, Kelly Search, which focuses on product and company directories. The tab on the far right is labeled "Web" and is essentially the Zibb equivalent of the Google default search. A Web search on Zibb, however, searches only industry vendors, standards bodies, trade associations, trade publications, and other relevant sites.

I encourage you to give Zibb a try. And please let me know what you think. If Zibb fails to turn up a site that should be in our database, I want to know. We want to hear both the bad news and the good. I believe that Zibb will save you time in your electronics-industry searches. But if it doesn't, tell us about it, so that we can try to make it better. EDN

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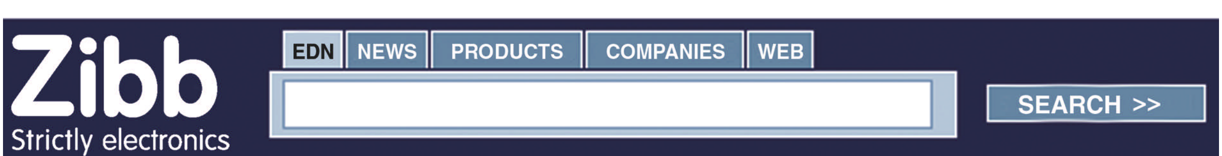

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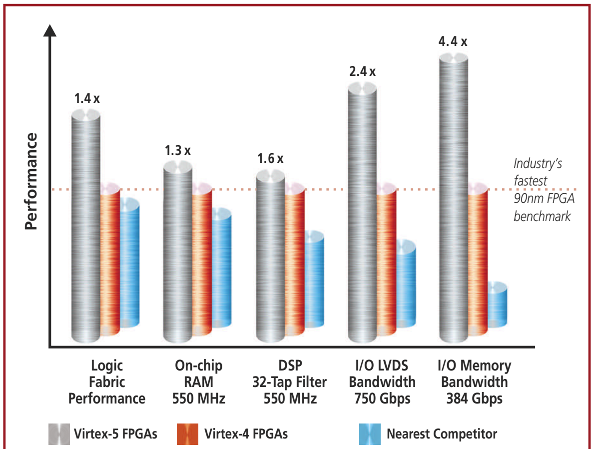

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DESIGN | idea

Improving Video Clock Generation in Modern Broadcast Video Systems

By Alan Ocampo, Applications Engineer

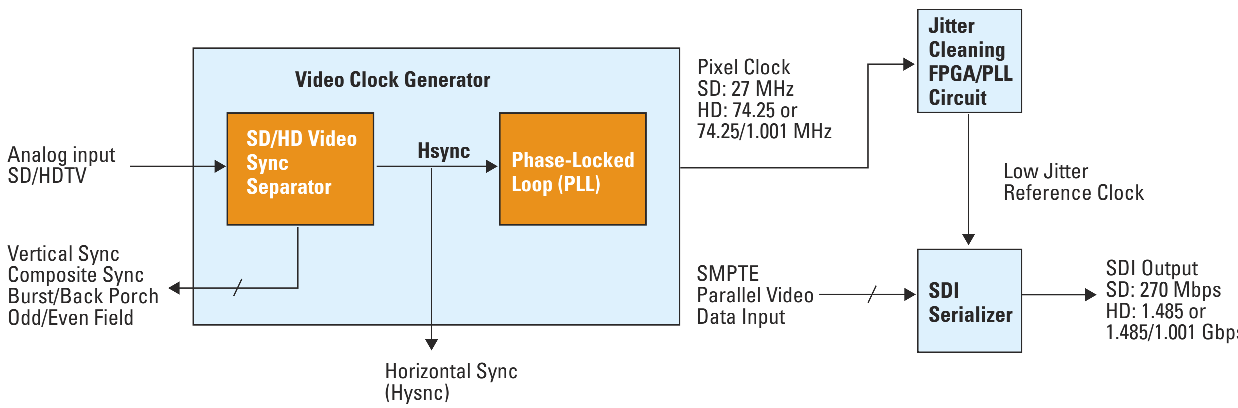

Figure 1. SDI Reference Clock Generator Block Diagram

The old adage "timing is everything" is well embodied in the modern broadcast studio, where precise timing of video clock and synchronization signals are essential to create, acquire, edit, and distribute analog and digital video. Today's broadcast systems must support industry-standard SD/HD formats, such as NTSC, PAL, 720p, 1080i, and 1080p, over analog and digital interfaces such as composite, component, and Serial Digital Interface (SDI). With high-speed SDI video equipment being increasingly used throughout the studio, improved video sync separation can more effectively produce video clocks with low jitter, which is crucial to meeting the stringent specifications of new SDI standards.

A video clock generator which generates various timing and clock signals from an analog video input consists of a video sync separator and Phase-Locked Loop (PLL). These two circuits are illustrated in the SDI application block diagram in *Figure 1*.

The video sync separator accepts a $1V_{p\text{-}p}$ analog video input with bi-level or tri-level sync and extracts the standard timing signals, such as Horizontal (Hsync), vertical, and composite sync, burst/back porch, and odd/even field outputs. To meet strict timing requirements of the latest HDTV standards, specifications such as HD tri-level sync separation, low output propagation delay, and 50% sync slicing are imperative. The latter ensures precise sync extraction by slicing at the proper 50% point of the bi-level or tri-level sync reference edges. This provides for improved Hsync jitter performance compared to non-adaptive, fixed-level sync slicing, even under irregular input conditions such as double or no 75Ω load termination or transmission loss. Hsync jitter is defined here as the peak-to-peak time variance in Hsync's falling-edge with respect to the input's sync reference-edge and is critical to the performance of the pixel clocks generated by the subsequent PLL block.

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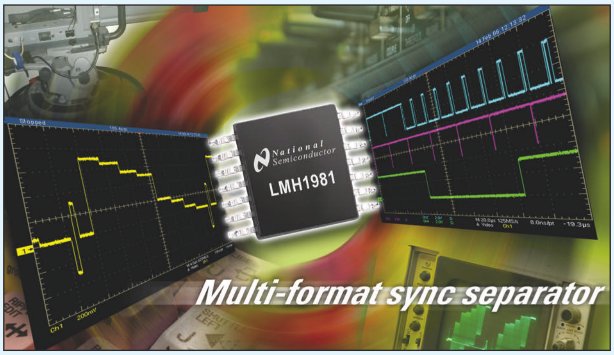
Multi-Format Video Sync Separator

The LMH1981 is a multi-format sync separator for high-definition broadcast and professional video systems. The device automatically detects the input video format and performs all the necessary sync separation to generate low-jitter horizontal and vertical sync signals for standard and high-definition video formats, including NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p.

The LMH1981 features the timing outputs needed for any video system, including horizontal, vertical and composite sync, odd/even field, burst/back porch clamp, and a patented automatic video-format detection feature. The device accepts both bi- and tri-level sync video inputs and features 50% slicing to ensure accurate separation of signals that vary in amplitude, offset, and noise. The device has a wide input range, allowing the inputs to accept video signals from 500 mV_{P-P} to 2 V_{P-P}.



Features

- 50% sync slicing
- Low jitter horizontal sync output
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video signals from 500 mV_{P-P} to 2 V_{P-P}
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns

The LMH1981 is ideal for use in a wide range of video applications such as, broadcast video equipment, video distribution, DTV and HDTV systems, and is available in TSSOP-14 packaging.

For FREE samples, datasheets, and more, visit
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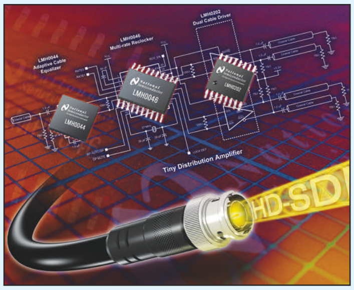
Adaptive Cable Equalizer



The LMH0044 adaptive cable equalizer is a monolithic integrated circuit for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 143 Mbps to 1.485 Gbps and supports SMPTE 292M, SMPTE 344M, and SMPTE 259M. This device implements DC restoration to correctly handle pathological data conditions (DC restoration may be bypassed for low data rate applications). The equalizer may be driven in either a single-ended or differential configuration.

Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation.

Features

- SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- High data rates: 143 Mbps to 1.485 Gbps
- Equalizes up to 200m of Belden 1694A at 1.485 Gbps or up to 400m of Belden 1694A at 270 Mbps
- 208 mW typical power consumption with 3.3V supply
- Manual bypass and output mute with a programmable threshold
- Single-ended or differential input
- Supports DVB-ASI at 270 Mbps
- 50Ω differential outputs
- Single 3.3V supply operation

The LMH0044 is ideal for SMPTE 292M/344M/259M serial interfaces, serial digital data equalization and reception, and data recovery equalization. The LMH0044 is available in LLP-16 packaging.

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Improving Video Clock Generation in Modern Broadcast Video Systems

The PLL block can generate one or more pixel clocks, which should be phase-locked to the leading-edge of Hsync, the PLL's reference input. To produce both SD and HD pixel clocks will require two PLLs, both designed to give the appropriate output frequency for any given Hsync frequency. Since the PLL derives a higher frequency pixel clock from a lower frequency Hsync, pixel clock jitter will be determined by different sources at different frequencies. Below the loop bandwidth, the clock jitter output by the PLL will be dominated by Hsync jitter, which can be a significant amount depending on the performance and quality of the sync separator. Above the loop bandwidth, it will be dominated by its PLL oscillator, typically a Voltage-Controlled Crystal Oscillator (VCXO) chosen properly for low phase noise and frequency tuning, among other characteristics.

In the block diagram, a pixel clock generator is used to derive a reference clock for an SDI serializer which receives SMPTE-compliant parallel digital video data and then encodes, serializes, and transmits uncompressed serial digital video over coax cable. A serializer requires a clean reference clock for its internal PLL to generate a bit rate clock that maintains the serializer and clocks its output bit-stream. If used to directly clock the serializer, any jitter on the reference clock could potentially transfer to the bit rate clock and consequently appear as SDI output jitter. As shown in ***Table 1***, SDI formats use increasingly high data rates and thus require clock sources with sufficient jitter performance.

For example, SMPTE 292M specifies the "timing" and "alignment" jitter requirements for an HD-SDI serializer's output bit-stream. Referring to the table, timing jitter should not be more than 1.0 UI[1] for jitter frequency components from B1 to B3, or 10 Hz to 1485 MHz, per SMPTE 292M. Alignment jitter—which is the high-frequency subset of timing jitter—should be no more than 0.2 UI from B2 (100 kHz) to B3. Outside of their respective frequency limits, both the timing and alignment jitter specifications roll off at 20 dB per decade. Output jitter above the jitter specifications can result in degradation of error performance at the SDI deserializer. Please see the SDI standards for more information.

The stringent jitter specifications of SDI standards demonstrate the profound need for a low-jitter pixel clock. In most cases, however, a generated pixel clock will have an intolerable amount of jitter, up to 6 ns_{p-p} for a typical SD pixel clock, which precludes direct application as a reference clock. Jitter reduction is therefore required to improve such unacceptable clock performance. The most common way to reduce pixel clock jitter is to use jitter-cleaning circuitry, usually implemented with additional Field-Programmable Gate Array (FPGA) or PLL stages. While jitter-cleaning circuitry is routinely applied by system designers, this can add significantly to component count, PCB area, power, and design cost and time.

A more effective way to reduce pixel clock jitter and thus improve SDI output jitter is to use a broadcast-quality video sync separator that has very low Hsync jitter, such as the LMH1981. This improved performance gives designers the flexibility to use smaller FPGAs or otherwise reduce jitter-cleaning circuitry and still produce an SDI output that complies to the jitter specifications.

Although broadcast systems are rapidly transitioning to high-speed SDI formats, the need to generate accurate video clocks from analog sources to process digital video data will be around for years to come. Current solutions require extensive jitter-cleaning circuits for generating an accurate reference clock to produce a SMPTE-compliant SDI output. However, the most fundamental and effective solution is to minimize jitter on the most critical timing reference, Hsync. This can only be accomplished using a high-performance analog video sync separator such as the LMH1981 in the clock generation signal path because, as we now know, timing is everything. ■

Access interactive broadcast video solutions diagrams at solutions.national.com

Table 1

Format	Standard	Bit Rate	Output Timing Jitter (B1 to B3)*	Output Alignment Jitter (B2 to B3)*
SD-SDI Standard- definition	SMPTE 259M, 334M	270 Mbps, others not widely used	1.0 UI[1] or 3.7 ns_{p-p}	0.2 UI or 740 ps_{p-p}
HD-SDI High-Definition; HD/SD-SDI Mulit-rate	SMPTE 292M	1.485 Gbps 1.485/1.001 Gbps	1.0 UI or 673 ps_{p-p}	0.2 UI or 135 ps_{p-p}
3-Gbps SDI up to 1080p/60 over a single link	SMPTE 424M	2.970 Gbps 2.970/1.001 Gbps	2.0 UI or 673 ps_{p-p}	0.3 UI maximum, 0.2 UI recommended

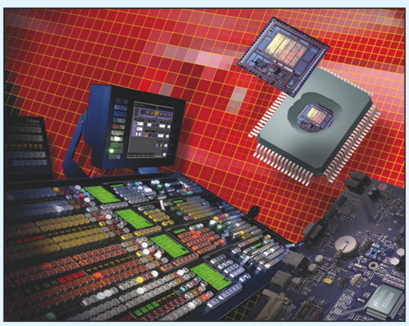
*B1, B2, and B3 are the jitter frequency band limits specified in the SMPTE standards.

[1]One UI, or Unit Interval, is equal to one bit period (1/bit rate) of the serial bit-stream.

Featured Products

Digital Video Serializer with Ancilliary Data FIFO and Integrated Cable Driver

The LMH0030 is a monolithic integrated circuit that encodes, serializes, and transmits bit-parallel digital video data. The serial data clock frequency is internally generated and requires no external frequency setting, trimming, or filtering components. The LMH0030 performs functions which include: parallel-to-serial data conversion, SMPTE standard data encoding, NRZ to NRZI data format conversion, serial data clock generation and encoding with the serial data, automatic video rate and format detection, ancillary data packet management and insertion, and serial data output driving.



Features

- SDTV/HDTV serial digital video standard compliant
- Supports 270 Mbps, 360 Mbps, 540 Mbps, 1.4835 Gbps, and 1.485 Gbps SDV data rates with auto-detection
- Low output jitter: 85 ps (typ), 125 ps (max)
- Low power consumption: 430 mW (typ) from 3.3V
- No external VCO required
- Fast PLL lock time: < 150 µs (typ) at 1.485 Gbps
- LVCMOS compatible data and control inputs and outputs
- 75Ω ECL-compatible, differential, serial cable-driver outputs
- 3.3V I/O power supply and 2.5V logic power supply operation

The LMH0030 SDTV/HDTV serial-to-parallel digital video interfaces for video cameras, VTRs, telecines, digital video routers and switchers, digital video processing and editing equipment, video test pattern generators and digital video test equipment, and video signal generators. The LMH0030 is available in TQFP-64 packaging.

For FREE samples, datasheets, and more, visit **www.national.com/pf/LM/LMH0030.html**

Digital Video Deserializer / Descrambler with Video and Ancillary Data FIFOs

The LMH0031 is a monolithic integrated circuit that deserializes and decodes SMPTE 292M, 1.485 Gbps (or 1.483 Gbps) serial component video data, to 20-bit parallel data with a synchronized parallel word-rate clock. It also deserializes and decodes SMPTE 259M, 270 Mbps, 360 Mbps, and SMPTE 344M (proposed) 540 Mbps serial component video data, to 10-bit parallel data. Functions performed by the LMH0031 include clock/data recovery from the serial data, serial-to-parallel data conversion, SMPTE standard data decoding, NRZI-to-NRZ conversion, parallel data clock generation, word framing, CRC and EDH data checking and handling, Ancillary Data extraction, and automatic video format determination.

Features

- SDTV/HDTV serial digital video standard compliant
- Supports 270 Mbps, 360 Mbps, 540 Mbps, 1.483 Gbps, and 1.485 Gbps serial video data rates with auto-detection
- Low power: 850 mW (typ)
- Uses 27 MHz crystal or clock oscillator reference
- Fast VCO lock time: < 500 µs at 1.485 Gbps
- Built-in self-test and video test pattern generator
- LVDS and ECL-compatible, differential, serial inputs
- 3.3V I/O power supply and 2.5V logic power supply operation

The LMH0031 SDTV/HDTV serial-to-parallel digital video interfaces for video editing equipment, VTRs, standard converters, digital video routers and switchers, digital video processing and editing equipment, video test pattern generators and digital video test equipment, and video signal generators. Operating over the commercial temperature range (0°C to +70°C), the LMH0031 is available in TQFP-64 packaging.

For FREE samples, datasheets, and more, visit **www.national.com/pf/LM/LMH0031.html**

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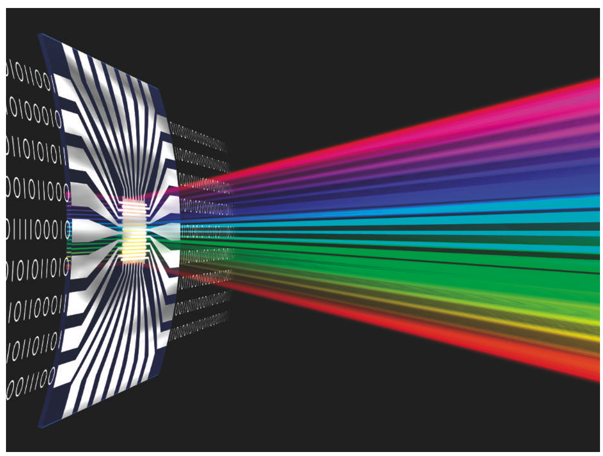
EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Organic semiconductors shine in LED/photosensor combinations

Silicon circuits provide high-speed switching of many tiny circuits and are good for use in small LEDs and photodiodes. Silicon has limitations, however, for systems that need to be cheap, environmentally friendly, disposable, and maybe even bendable. Organic circuits, on the other hand, excel in these areas. Incorporating technology whose developers ultimately won the Nobel Prize in chemistry in 2000, these circuits comprise a conductive-polymer compound that manufacturers can apply in a thick-film process with the same technology that ink-jet printers use.



The organic-semiconductor-based Photonics Solution Platform offers spectral-sensitivity ranges from infrared through the visible-light spectrum, depending on the formulation of the organic material, which also determines the photodiodes' dark current and dynamic range.

Organic semiconductors will not replace silicon because they're not particularly fast and they don't support the fine-line geometries of silicon. However, they bear watching if you want inexpensive, perhaps disposable, or large-area LEDs or photosensors.

Klaus Schroeter, chief executive officer of Austrian start-up Nanoident, says that a common OLED (organic-LED)—at 5×5 mm—is too big to be practical in silicon, but, he claims, is cheap and easy with organics. OLEDs are already finding use in displays for embedded systems. Organic devices are also intriguing for use in image sensors because, just by changing the voltage polarity on an OLED, you can change it from a light source to a light sensor. For example, you could integrate a fingerprint sensor into a display: If you touch the display, you can verify not only the fingerprint, but also the finger's hemoglobin count, verifying the fact that the finger is alive and thereby foiling the authors of numerous movies and books whose bad guys trick identification units with severed body parts.

Nanoident claims to be the first to develop organic-semiconductor-based optoelectronics. The company's new Photonics Solution Platform allows you to design image sensors combining LEDs, photosensors, and simple IC functions, such as amplifiers. You can start with either a discrete or an array-based photosensor, add an LED array for an illumination source, and top it off with any necessary amplifiers or simple decision-making logic. If you need serious number-crunching ability, you can add a conventional microprocessor chip onto the sensor. Work up the sensor design in collaboration with Nanoident, and the Photonic Solution Platform delivers the circuit design and component parameters. Nanoident then prints the circuit, including components, on surfaces such as foil, glass, paper, and pc boards.

The display resolutions range from 250 to 1000 dpi. The spectral sensitivity ranges from infrared through the visible-light spectrum, depending on the formulation of the organic material, which also determines the photodiodes' dark current and dynamic range. A representative price for a fingerprint-swipe sensor for a high-volume consumer product, such as a cell phone, is less than $2.

Organic semiconductors even offer a "green-power" hook: Photovoltaics are close relatives of photodiodes, and several companies, including Nanosolar (www.nanosolar.com) and Konarka Technologies (www.konarka.com), are working to exploit the cheap-production aspects of organics. Although organic devices are currently about an order of magnitude or so less efficient than silicon-based photovoltaics, organic photovoltaics are so cheap to manufacture that the low cost of ownership and the rapid payback period more than offset their relative inefficiency.

—by Margery Conner

▷**Nanoident**, www.nanoident.com.

Chip offers authentication, protection to single-cell battery packs

Cell-phone battery gauges are neither accurate nor consistent: The battery-charge symbol seems to relate only coincidentally to battery charge, causing users to charge their phones when they don't need to, consequently reducing battery life. However, as the newest generation of cell phones moves into a more intensive data-usage model, service providers are demanding that battery packs have more intelligence. They fear that counterfeit battery packs will explode in phones carrying the providers' brand names, making them liable to expensive lawsuits. Meanwhile, some users suggest that vendors are requiring battery authentication to protect themselves from after-market battery-pack sales (see the online Feedback Loop for "Friend or foe: Battery-authentication ICs separate the good guys from the bad," *EDN*, Feb 2, 2006, pg 59, www.edn.com/article/CA6301616).

However, Brian Rush, business manager for Maxim's fuel-gauge line, disagrees with these users' viewpoint. Service vendors, such as Verizon (www.verizon.com), are liable in a battery-related accident, he says, so they are pressuring equipment vendors to provide battery authentication. In addition, both equipment and service vendors want to preserve their brand integrity. So, Maxim and other vendors are setting the stage for a new generation of fuel gauges targeting one-cell battery packs in cell phones. Maxim claims that its new DS2790 fuel gauge is the first single-chip approach offering accurate battery-fuel-gauge and protection circuitry for single-cell packs.

The circuitry precisely measures current, accumulated current, voltage, and temperature, and it runs your cell-phone manufacturers' proprietary fuel-gauge algorithms on its internal 16-bit MAXQ microcontroller. The DS2790 contains 16 kbytes of program memory, which includes 8 kbytes of password-protected EEPROM and 8 kbytes of ROM; 128 bytes of data EEPROM for storing data such as charge parameters, cell characteristics, and manufacturing data; and 512 bytes of data RAM. The ROM contains routines that allow reprogramming over the I^2C interface, SHA (Secure Hash Algorithm)-1 authentication, and support for in-circuit debugging. Rush claims that hackers can too easily break simpler authentication codes, so equipment vendors need the complexity of SHA-1. The product is available in 28-pin TSSOP and TDFN packages with prices starting at $2.50 (1000).**—by Margery Conner**

▷**Maxim**, www.maxim-ic.com.

FROM THE VAULT

"The development of sophisticated design techniques and relatively standard manufacturing processes will permit fabrication of relatively small quantities of truly custom designs (ICs) at attractive costs. During the 1970s, a major shift to custom designs will occur, necessitating a substantial change in vendor-supplier relationships."

Jack Kilby, assistant vice president and manager of the customer-requirements center at Texas Instruments' Components Group, *EDN*, Jan 1, 1970

DILBERT *By Scott Adams*

07.20.06

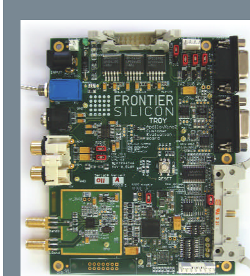
Kit eases mobile-TV design

Frontier Silicon's latest evaluation kit allows designers to test and measure the performance of the company's Apollo RF receiver and Kino 2 chip set for mobile-TV applications. The Troy kit receives a T-DMB (terrestrial digital-multimedia-broadcasting) RF signal on Band III and the L Band and delivers an MPEG-2 transport stream to a host processor for audio and video decoding. Troy can simultaneously process as many as four T-DMB streams and display each one in a separate player window on the PC.

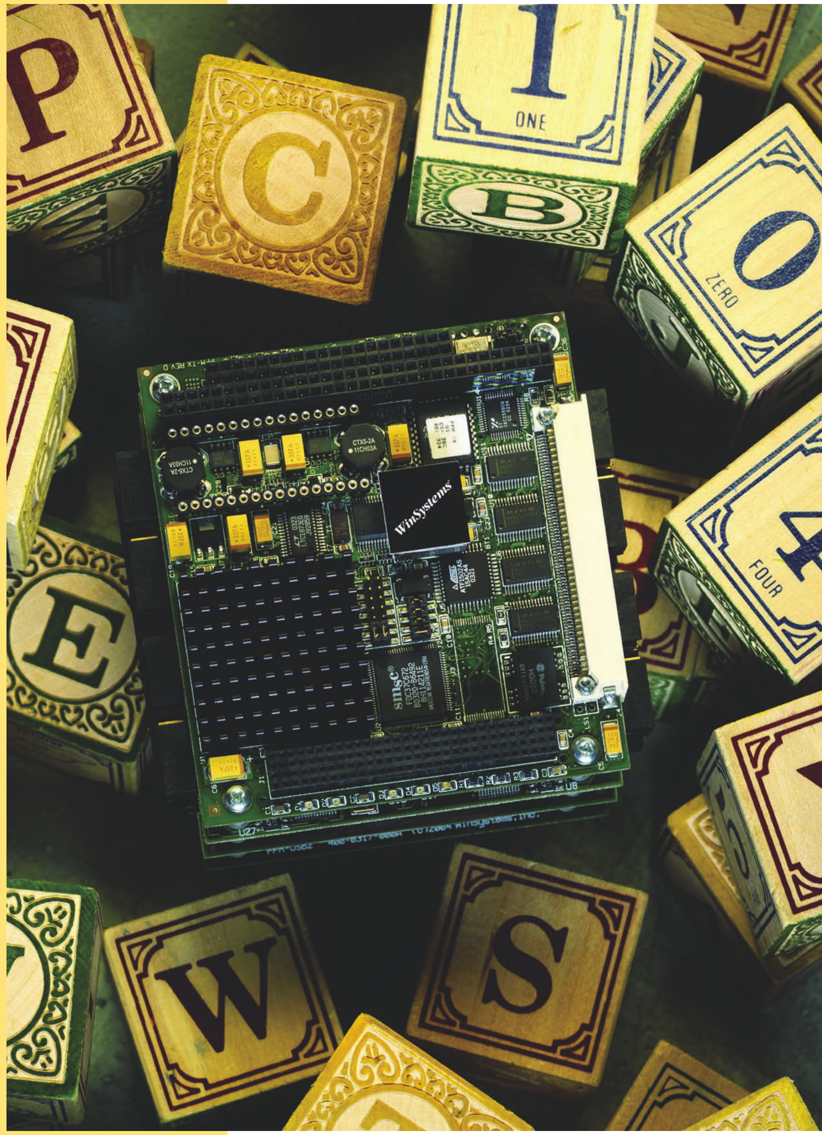
Although the kit allows a standard PC to act as the host processor, the interface connector supports multiple supply voltages and signals for connection to all popular media-processor-development kits. Available now, the Troy evaluation kit sells for $1400.

—by Warren Webb

▶**Frontier Silicon**, www.frontier-silicon.com.



A new evaluation kit allows designers to measure the performance of Frontier Silicon's multistandard mobile-TV chip set using a desktop PC.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SRIO switch for base stations adds preprocessing function, algorithms

The architecture of cellular base stations typically involves a bank of RF front-end cards that sends packetized sample data, generally through SRIO (serial RapidIO) to an ASIC or FPGA. The ASIC or FPGA acts as a fairly simple switch, routing the packets to a waiting bank of DSPs and control-plane processors at the direction of the control plane. This arrangement begs for an off-the-shelf SRIO switch to form the hub of the processing backplane. Filling this need, IDT has announced a product that adds functions to the switch chip.

The company examined the processing tasks that the DSP chips and fabric's chip-rate hardware were performing and found commonly occurring tasks during the transmitting and receiving operation. Both in-sample data manipulation, such as sign extension and endian conversion, and multipacket operations, such as multicasting, reordering of samples, and summation across samples, occur. Some of these operations occur in the high-speed chip-rate processing hardware, and some occur in the symbol-rate operations on the DSP chips. Because these operations are relatively standard, remain constant with time or context, and occur with some frequency, IDT moved them from the chip- and symbol-rate hardware into dedicated hardware inside the switch chip.

According to IDT Senior Product Manager Bill Beane, when you present this scenario to the base-station design team, the hardware engineers typically want to know the resulting aggregate data rate. The software-team leaders, however, want to know about the offload capability. Anything routine that they can move from DSP code means more code space and more execution time for the more complex operations.

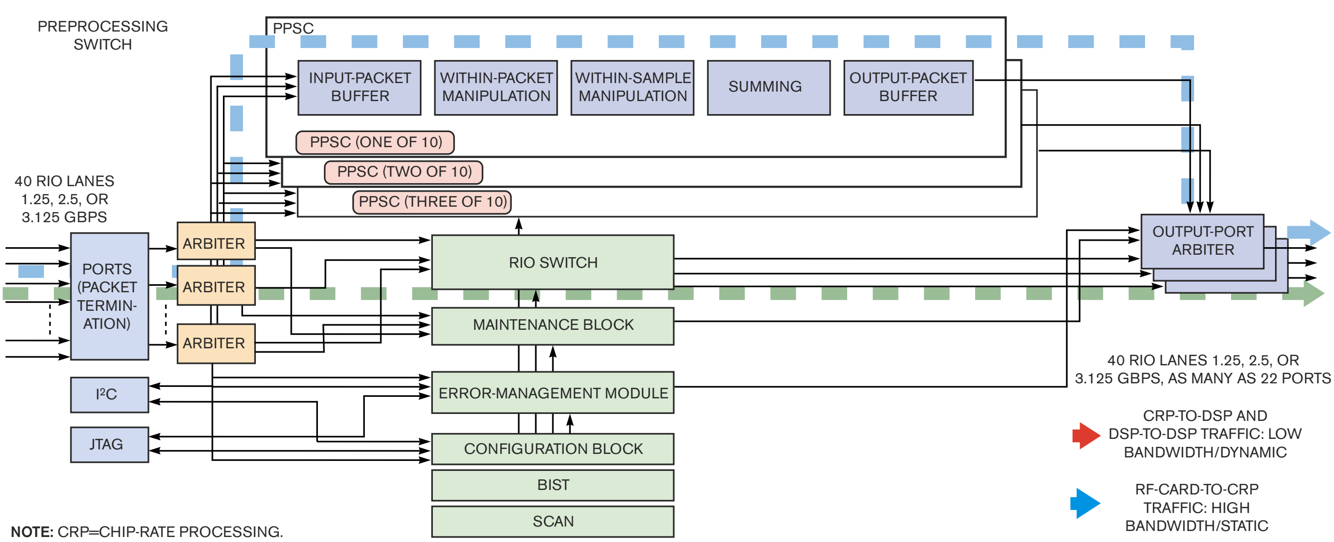
As a result, IDT announced an SRIO switch chip. The chip supports 40 SRIO lanes at speeds as high as 3.125 Gbps each. You can group the lanes in clusters of four, and you can configure the drivers to support either chip-to-chip or backplane-SRIO interconnections. The chip also supports SRIO-standard priority and queuing algorithms to manage data flow in what can become complex multichip conversations. The chip also supports the standard's error-management and -maintenance functions.

The competing needs for performance, small die, and manageable power dictated a mesh configuration for the switch fabric. Power depends on the usage scenario. Beane says that much of the design effort went into modeling processing topologies and algorithms and examining the data flow and power consumption for each. The offloaded processing tasks occur in a block that is parallel to the switch fabric, between banks of input and output arbiters. The block comprises 10 identical register-programmed state machines; input and output buffers surround these machines. Each state machine can perform in-sample, multisample, and summing operations, and all 10 machines can operate in parallel.

The result is a repartitioning of the tasks in a typical base-station-processing system. This task is neither trivial in itself, nor trivial in its implications for the packet-processing software team. Consequently, IDT this month will provide an Advanced Mezzanine Card-profile reference design that will include a full, production-capable evaluation board with four Texas Instruments (www.ti.com) Himalaya DSPs and a latency-accurate simulator. The IDT 70K2000Z is available for sampling now, and production will begin in November. Price is approximately $125 (10,000).

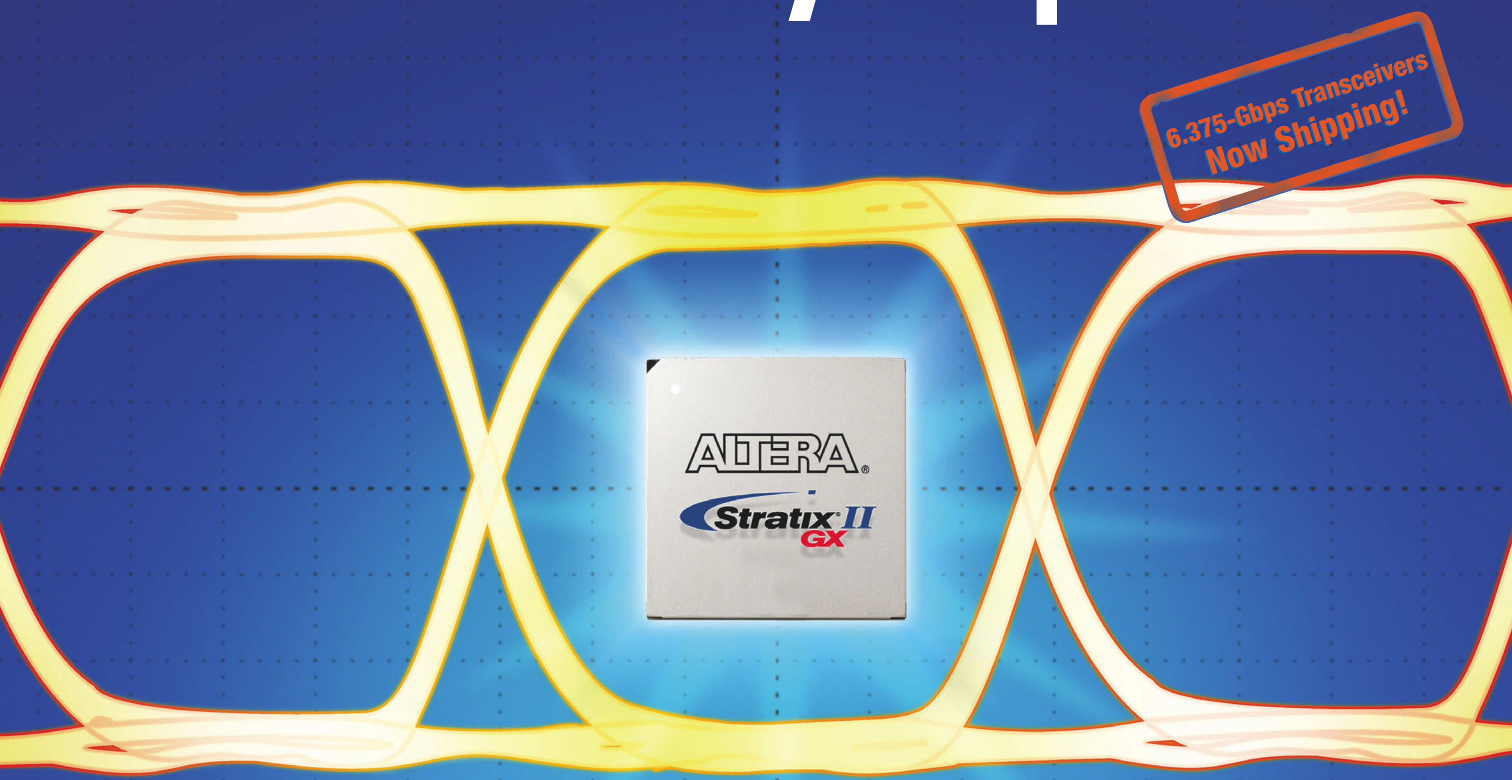
—by Ron Wilson

▷**IDT**, www.idt.com.



IDT's intelligent 70K2000Z combines a 40-port SRIO mesh switch with significant offload-processing capability for both chip- and symbol-rate tasks.

The FPGA Eye Opener!



Transmit eye diagram at 6.375 Gbps. For characterization details, see www.altera.com/stratix2gx/characterization.

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GLOBAL DESIGNER

Partners drive WiMax momentum across Asia

Since early in the development of the WiMax wireless-broadband standard, pundits have predicted a lot of deployment in regions such as Asia where large geographic areas lack a wired infrastructure. That scenario is coming true, and chip vendors in North America, Europe, and other regions continue to partner with system and telecommunications OEMs in the target regions. Just recently, OEM Tata Elxsi in Bangalore, India, signed on with Texas Instruments in an IEEE 802.116e mobile-WiMax initiative. Meanwhile, UK-based picoChip has found another Chinese partner for its WiMax silicon.

The TI/Tata Elxsi partnership intends to provide telecom-equipment vendors with an accelerated path to mobile-WiMax-base-station development. Tata Elxsi has developed 802.16e MAC (media-access-control)-software IP (intellectual property) that it will meld with TI's TMS320TCI6482 DSPs. The companies based the reference design on Mercury Computer's MTI-203 AMC (Advanced Mezzanine Card), and end systems will likely rely on the ATCA (Advanced Telecom Computing Architecture) standard for building modular communication systems. The partnership is key because Tata Elxsi offers both the wireless-domain experience in technologies such as the MAC and the system-design experience, along with relationships with target equipment vendors.

Meanwhile, picoChip continues to push its programmable-silicon architecture into all WiMax flavors. The latest partnership is with Chinese telecom OEM China GrenTech. The company brings significant RF- and power-amplifier experience, along with manufacturing capability, to the partnership. China GrenTech has been a player in the 3G-cellular market, and the picoChip partnership will allow quick entry into the WiMax market.

—by Maury Wright

▷**China GrenTech**, www.powercn.com.
▷**Mercury Computer**, www.mc.com.
▷**picoChip**, www.picochip.com.
▷**Tata Elxsi**, www.tataelxsi.com.
▷**Texas Instruments**, www.ti.com/wimaxwi.

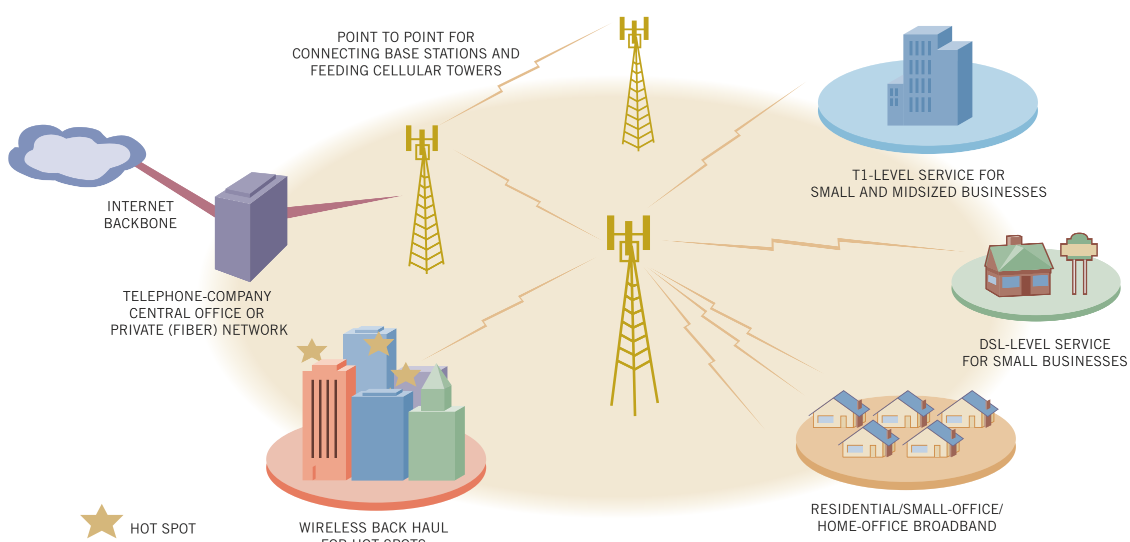
Ceramic substrate enables distributed processing in vehicles

07.20.06

The automobile has evolved to depend on a complex distribution of computational resources in subsystems ranging from brakes to safety to engine control. But distributing processor-based subsystems into environmentally challenging locations within a vehicle remains a problem. Japan-based Kyocera has just demonstrated an ECU (engine-control unit), which it deployed directly in an automatic transmission from Aisin AW Co. Locating the ECU on the high-torque, six-speed transmission exposes the subsystem to harsh temperatures and vibration. Kyocera developed a multilayer-ceramic substrate that could both handle the harsh environment and deliver on the reliability and small footprint that automakers need. Kyocera recently demonstrated the ECU at the Automotive Engineering Exposition 2006 in Yokohama, Japan.

–by Maury Wright

▶**Aisin AW Co**, www.aisin-aw.co.jp.
▶**Kyocera**, www.kyocera.com.



WiMax will serve as an alternative to T1 for businesses, as an alternative to DSL for cable and consumers, and as a back-haul option for cellular base stations and hot spots.

Blackfin is at 32°54.6 N, 96°45.1 W

▶ Maxtrack MTC-600 Vehicle Tracking System

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ANALOG DEVICES

RESEARCH UPDATE

BY MATTHEW MILLER

Researchers prepare to test the condition of a wiring bundle in the cockpit of a retired Boeing 737.

Sparks could prevent airline crashes

Airline-maintenance crews, not to mention passengers, face a frightening prospect: Somewhere within the miles of wiring inside a commercial airplane, a minuscule physical fault, such as a bit of worn insulation, can cause a catastrophic short circuit. For example, investigators fingered faulty wiring as the cause of a fire that led to the crash in 1998 of Swissair Flight 111, which killed 229 people when it went down off Nova Scotia.

Now, researchers at Sandia National Laboratories have announced a technology that could make it easier for airlines to locate and repair such faults. The suitcase-sized PASD (pulsed-arrested-spark-discharge) system uses high voltage to propel a nanosecond-long pulse of electricity through as many as 40 wires at a time. Due to the high voltage, the pulse readily jumps from any gap in faulty insulation to the aircraft bulkhead or another faulty wire nearby, causing a spark. The pulse is so short that it cannot do any damage, and the system measures current-return time to pinpoint faults to within inches.

Astronics Advanced Electronic Systems (www.astronicsaes.com) has licensed the technology and plans to offer it commercially starting in September.

▷**Sandia National Laboratories**, www.sandia.gov.

Researchers listen to the sounds of CMOS

Scientists at NIST (National Institute of Standards and Technology), working with IBM and RF Micro Devices, have developed methods to reliably measure the faint thermal noise generated by the random motion of electrons in CMOS transistors. Characterizing this noise allows engineers to better tune systems, such as cellular phones, for optimal signal range, data rate, and battery life, according to NIST. The methods involve measuring the noise on the wafer before cutting and packaging.

The group also detailed its ability to perform "reverse" noise measurements, which focus on the noise that transistor inputs emit when they reflect and scatter incoming signals. This information can help engineers discover the impedance properties that will best minimize noise, according to NIST.

▷**National Institute of Standards and Technology**, www.nist.gov.

▷**IBM**, www.ibm.com.

▷**RF Micro Devices**, www.rfmd.com.

07.20.06

Molecular electronics gel in a jar

Researchers from Philips Research and the University of Groningen (Groningen, Netherlands) have developed a molecular self-assembly process that reliably produces arrays of 1.5-nm-thick molecular diodes on standard substrates. Previous attempts to build such structures, which feature a single layer of molecules sandwiched between gold electrodes, have suffered from shorting. In this process, an additional plastic electrode layer prevents shorts.

Not a week goes by these days without some research outfit touting an advance in self-assembling, nanoscale circuitry. The Philips/Groningen team, however, claims that its work stands out because it will allow reliable, reproducible measurements of molecular junctions–an essential step in studying the potential applications of such circuits.

▶**Philips Research**, www.research.philips.com.

▶**University of Groningen**, www.rug.nl.

Dutch researchers have concocted a high-yield process for producing molecular diodes.

Blackfin is spinning

▶ Denon DN-S3500
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- GCC/Linux
- Cryptography
- Rights Management
- Open Source
- Car Telematics
- IPTV

Scratch vinyl goes digital

Professional DJs gave Denon a special request: "We want to play MP3s with all the features of our vinyl rigs, including scratch, reverse, brake, filter, and flanger." But enabling these user control needs, coupled with near-zero latency of audio encoding and decoding, required a unique 32-bit processor. So Denon cued up Blackfin®. With 800 MMACS performance at $5 cost, Blackfin scratched the competition. Now Blackfin is everywhere, bringing the beats.

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ANALOG DEVICES

Painting microprocessors in broad strokes

No one likely would argue the microprocessor's place on our roster of Milestones That Mattered. Surely, there'd be heated discussion over who invented the processor. But the benefits of the invention are clear. Productivity has benefited hugely from the processor-based PC. And thousands of processors surround us in our everyday lives, with vendors adding more daily.

One of the themes of our 50th anniversary issue, due this September, will be "softwarerization." We know it's not a word. But the movement of functions to software has been an unmistakable and enduring trend, which the microprocessor, at least in the broadest set of applications, has enabled. Designers can implement anything from simple hardware circuits, such as UARTs, to complex data-coding functions, such as MPEG, in software.

But let's get back to history. Intel claims to have developed the first commercial microprocessor with the launch of the 4004 in 1971. The company built the first design for customer Busicom of Japan and targeted calculators, although Intel later reacquired the rights to the 4004. Ted Hoff and Federico Faggin of Intel get the credit, although Intel tried at one point to erase Faggin's contribution from history after he defected to Zilog.

Some historians, however, believe that Four Phase Systems was shipping the AL1 processor a year before Intel delivered the 4004. Lee Boysel designed the AL1, but history largely buried the achievement because Motorola acquired the company, which most people forgot about. Texas Instruments also lays claim to early processor development.

What's undeniable is that Intel was most successful in commercializing the technology that would underwrite decades of innovation. You can read the complete original *EDN* account of the 4004 with the online version of this article at www.edn.com/060720mtm. That early processor sold for $100 in low volumes. EDN

01.15.72

FROM THE VAULT

"Announcing a new era of integrated electronics."

This introduction for a new IC may seem immodest, but Intel Corp. might just be correct. The IC is a single-chip CPU designed for low-speed microprogrammable applications, such as terminals, peripherals, test systems, and process control. The one-chip CPU was described at the *EDN*/EEE seminars in August.

The CPU, Type 4004, is designed to work with other members of Intel's MC5-4 microcomputer set. The other ICs in this kit of standard building blocks are the 4001 ROM, 4002 RAM, and the 4003 shift register (SR).

The minimum system configuration consists of one CPU an one 256×8-bit ROM. For one-of-a-kind applications, an electrically programmable ROM can be used in place of the mask-programmable 4001. The MCS-4 microcomputer is fabricated with silicon-gate, low-threshold MOS technology.

Packaged in a 16-pin ceramic DIP, the CPU chip consists of a 4-bit adder, a 64-bit (16×4) index register, a 48-bit (4×12) program counter and stack, an address incrementer, an 8-bit instruction register and decoder, and control logic. Forty-five instructions are included in the 4004's repertoire. All timing, control, and arithmetic operations are implemented internally.

Information flows between the 4004 and the other chips through a four-line data bus. A system built with the MCS-4 set can have up to 4k×8-bit ROM words, 1280×4-bit RAM characters, and 128 I/O lines without requiring any interface logic. With the use of external gates, the computer size can be increased even further. The MCS-4 uses a 10.8-μsec instruction cycle. The basic instruction execution requires eight or 16 cycles of a 750-kHz clock. Addition of two 8-digit numbers requires 850 μsec.

Custom systems using this 4004 chip are implemented by microprograms stored in a ROM. The idea of microprogramming a process to implement a special controller is not new. IBM's system 360 computer and HP's 2100A desk calculator are two examples of both large and small systems that have exploited the inherent design and production advantages of microprogramming. In desktop calculators, about 35% of the logic is associated with doing arithmetic. The other tasks are keyboard encoding, printing results, displaying status and general control. These functions can be done by microprogramming rather than by additional random logic. Microprogramming can even be used for keyboard switch debouncing and for converting 4-bit BCD code to seven-segment lamp code. Many features may be added to systems using this chip by providing additional ROMs.

This approach provides a flexible and modular technique for system design in which memory devices are used instead of logic devices. The major limitation to its application is speed. While an IC logic can make a decision in about 5 nsec, and combinatorial networks allow many decisions to take place in parallel, this computer chip performs decisions sequentially at 10.8 μsec per instruction.

—*EDN*, Jan 15, 1972

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Paragon / B. Braun – The Challenge

The processor used in Paragon OEM customer and medical device maker B. Braun Medical's product was about to be obsolete; with demand still strong, Paragon needed to replace the main processor while minimizing changes to the circuit board. This revision would need to be made quickly: B. Braun's supply of processors was rapidly dwindling and, at the same time, the FDA would need to review and approve any new design to the product. These were heart stopping challenges confronting Paragon. Enter Avnet.

Avnet EM and Atmel – The Solution

Avnet and Atmel Corporation engineers studied the B. Braun board, in search of the right ARM solution to replace the obsolete microcontroller, while seeking opportunities to help Paragon improve overall performance, efficiency and cost-effectiveness on the project. On the technical side, Atmel came through with their feature rich ARM9 Smart Microcontroller. Avnet then supported the program on the supply chain side, keeping Paragon informed on the latest pipeline issues as it readied for production. During the entire process, neither Avnet nor Atmel missed a beat, and it really paid off for Paragon.

For additional application solutions and to download the case study, visit: www.em.avnet.com/atmel/satb

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Scaling: a balanced view, part three

In the last installment of Analog Domain, the application's matching, noise, and 1/f noise requirements determined the model minimum circuit's load capacitance, C_{MIN}—a representation of the following stage's input impedance. Matching varies in inverse proportion to $1/L_{MIN}$; noise and 1/f noise follow an inverse-square-law relationship with the minimum length (**references 1** and **2**).

For example, for applications in which matching constrains the dynamic range, such as track-and-hold amplifiers and several ADC architectures, you can express the offset voltage, V_{OS}, as

$$V_{OS}=\frac{n_\sigma \gamma T_{OX}}{\sqrt{WL}}.$$

Here, n_σ is the number of sigmas that your company's yield model requires, γ is a process-dependent parameter, T_{OX} is the gate-oxide thickness, and W and L are the device width and length.

The gate capacitance, C_{GATE}, of the transistors that must meet the matching requirements is

$$C_{GATE}=\frac{\varepsilon_0 \varepsilon_R WL}{T_{OX}},$$

where ϵ_0 is the permittivity of free space and ϵ_R is the relative permittivity of the gate oxide. Combining these two equations gives the C_{MIN} of the transistors that satisfies the matching requirements:

$$C_{GATE}=\varepsilon_0 \varepsilon_R n_\sigma^2 \gamma^2 T_{OX}\frac{DR^2}{V_{SIG(RMS)}^2},$$

where DR is the application's matching-limited dynamic-range requirement. Due to the strong influence that matching requirements have on C_{MIN} and, as a result, dissipation, circuits that demand tight matching between large numbers of transistors often make use of circuit techniques, such as offset cancellation, that reduce the requirements for individual devices.

In applications for which white noise limits the dynamic range, including a broad class of small-signal amplifiers, converters, and filters,

$$V_{NOISE}^2=\frac{kT}{C_{NOISE}},$$

though recent efforts suggest methods that beat this traditional floor. Expressing this limit as a minimum capacitance, with dynamic range as a parameter, yields

$$C_{NOISE}=kT\frac{DR^2}{V_{SIG(RMS)}^2}.$$

After determining the load capacitance necessary to meet dynamic-range requirements, the next step is to calculate the current necessary to sufficiently drive this capacitance to meet the application's ac specifications—bandwidth, settling time, slew rate, and total harmonic distortion.

Fundamental to these measures is the MOSFET's transconductance, gm:

$$gm=\frac{2I_D}{V_{GT}},$$

where $V_{GT}=V_{GS}-V_T$ in strong inversion and

$$V_{GT}=\frac{2nkT}{q}$$

in weak inversion. Bandwidth, the ratio of the unity-gain frequency, F_0, to the dc gain, A_0, follows from the transconductance and gate capacitance:

$$BANDWIDTH=\frac{F_0}{A_0}=\frac{gm}{2\pi A_0 C_{GATE}}.$$

In certain applications, meeting the application's bandwidth requirements is not insufficient; designs must prevent slew-rate limiting, which can impose another requirement on the minimum current:

$$I_{SR}=2\pi F_{SIG} V_{SIG} C_L.$$

Similar equations describe the minimum current necessary to attain specific second- and third-harmonic-distortion levels with and without feedback. For these, refer to **Reference 2**.

As was the case with the voltage efficiency, the model requires an assumption of current efficiency, η_c. Given a differential-signal path—a practical departure from the single-transistor string under discussion thus far—and modest current scaling in the bias-current mirror, an η_c of one-third is a good, if somewhat conservative, starting assumption for current efficiency of a single stage. In practice, common circuit-design practices more efficiently distribute bias currents, but the precise number depends upon both bias-generator and signal-path-circuit topologies.

The sum of string currents—or, in the case of differential circuits, the half-circuit currents—multiplied by the current efficiency yields the supply current, I_{DD}. The product of supply current and supply voltage, which you calculated from the application's signal-swing requirements, results in the minimum power dissipation necessary to attain the originally stated parametric goals. EDN

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References are available at www.edn.com/060720ji.

Joshua Israelsohn is director, technical information at International Rectifier Corp. You can reach him at edn-joshua@mindspring.com.

BY HOWARD JOHNSON, PhD

Reference-free pair

A correspondent from Capstone Visual needs to carry some high-speed network traces across his two-layer pc board. The board consists of 62-mil-thick FR-4 material. No solid plane layer exists anywhere on this board.

To manage skew between the two traces, my correspondent routed them exactly on top of one another—one on the top layer and one on the bottom. He needs a way to calculate the trace width necessary to make a good 100Ω differential configuration using this geometry.

Before I address this issue, I should congratulate my correspondent for recognizing that *any* trace configuration with a uniform cross section makes a perfectly good transmission line. You can use one trace with a solid reference plane, two traces side by side, two traces above and below one another, or four traces in a quad configuration; the possibilities are endless. Just keep the geometry consistent, and then all that matters are the impedance, delay, attenuation, and crosstalk.

My correspondent's traces are short compared with the extent of his network connection, so the trace delay and trace loss are immaterial.

Regarding the differential impedance, you can use an "image-plane" method to calculate the impedance of that configuration.

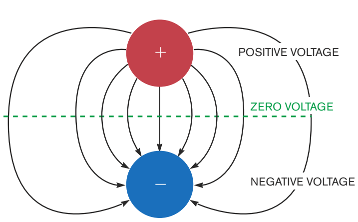

Figure 1 A zero-voltage plane bisects every symmetric differential configuration.

To calculate the impedance of an above-and-below differential-pc-board-trace setup with no reference plane, just lie to your 2-D field solver.

Figure 1 shows a cross-sectional view of two round conductors, assuming an air dielectric. (The conductors need not be round; any shape gives the same type of picture.) The electric-field patterns in the region surrounding the traces emanate from each trace perpendicular to its surface. A lot of lines flow directly from the positive trace to the negative trace. The lines bulge on either side. Voltages at the top of the drawing are positive, and voltages at the bottom are negative. Everywhere along a line drawn through the middle they are *exactly* 0V.

The dotted, green horizontal line bisecting the diagram represents an imaginary plane, or image plane, separating the two conductors. "Symmetry" in this case means that, if the differential pair is properly balanced, the voltage everywhere on the image plane remains zero at all times. Therefore, concerning the differential mode of propagation, no circuit can distinguish between, first, the original unreferenced configuration and, second, the same configuration with a real, physical, 0V reference plane added in the middle.

To calculate the impedance of an above-and-below differential-pc-board-trace setup with no reference plane, just lie to your 2-D field solver. Tell it that there is a solid reference plane dead center in the middle of the stackup. Separately compute the impedance from the top trace to the plane (a normal microstrip arrangement) and double that number to get the complete differential impedance.

The image-plane method makes quick work of the impedance calculation, but what about crosstalk? Lacking a solid reference plane, my correspondent's traces will be particularly sensitive to crosstalk from nearby sources. His circuit may not function for crosstalk reasons, but at least it won't suffer reflections! EDN

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Go to www.edn.com/060720hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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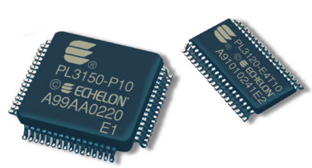

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Sweating blood over hardware-interface routines

In the 1980s, I obtained a number of consulting contracts to put the Vinten aerial photo camera and various other sensing devices into fixed-wing and helicopter aircraft. Along the way, I developed a computer-control system for the cameras that would adjust the trigger interval to obtain the desired overlap from frame to frame. It used a Commodore 64 with modified video-overlay circuitry.

One of these jobs was for a government agency in Edmonton, AB, Canada. There was a lot to do. The cameras and sensors went into a pod on the bottom of a Jet-Ranger helicopter. A rack of control equipment mounted on seat rails in the cockpit. The entire system was dual-powered from 117V-ac or large gel-cell batteries.

The system came together in the workshop just days before we were due to ship it. All the subsystems worked correctly, so we moved on to operating the complete system. It ran flawlessly for an hour or so, the cameras triggering correctly every few seconds. Then, in one of those heart-stopping moments that every engineer has experienced, an anomaly: The cameras fired off a burst of frames at high speed and then returned to the original interval.

The Vinten camera draws 20A for a few milliseconds every time it starts, so it's a major source of electrical noise. I had carefully designed the electronic interface between the computer and the cameras to minimize the effect but, I thought, maybe not carefully enough. The computer interface was an input/output shift-register pair attached to the parallel port. The shift-register parallel connections drove the camera relays, read back the radar altimeter, recorded video ground speed, and controlled other devices. I spent days peering into my scope, looking for noise spikes. Nothing showed. I installed various noise-control circuits, but the problem recurred at random.

Delivery was now late. The client insisted that the hardware appear in Edmonton. Reluctantly, I advised him of the problem—promising that I'd find it eventually—and shipped everything off. A week passed, and I still had no idea where to look.

The time came to fly to Edmonton. I packed every diagnostic tool I owned and headed out to the airport for a morning flight. Then, as we were watching the in-flight movie—*Back to the Future*—it came to me.

In Edmonton, the client was not happy. I sat down with the equipment, typed in two lines of assembly code, and held my breath. The system operated perfectly.

The problem: Two software routines were accessing the interface hardware. One routine, to read the ground speed, was part of the main loop. Another routine accessed the interface as part of the 60-Hz timing interrupt. Normally, these routines didn't get in each other's way. However, if the main-loop routine was reading the ground speed when a 60-Hz interrupt occurred, it would resume with corrupted ground-speed data, which then misadjusted the camera interval. The solution: Two instructions to disable the 60-Hz interrupt while reading ground speed.

This experience taught me that it's asking for trouble to access hardware from more than one point in the program. There should be a single interface routine that controls access to the hardware. Furthermore, it's important to realize that any section of the code can be interrupted and may corrupt the system state. To prevent this situation, you need to disable and enable interrupts or save additional state as part of the interrupt-service routine. This type of problem is nasty to debug, because it occurs at random intervals. So, you must properly engineer the system.

Testing and test equipment don't always help. As the saying goes, sometimes you have to think about it until little drops of blood appear on your forehead; then, it will come to you. **EDN**

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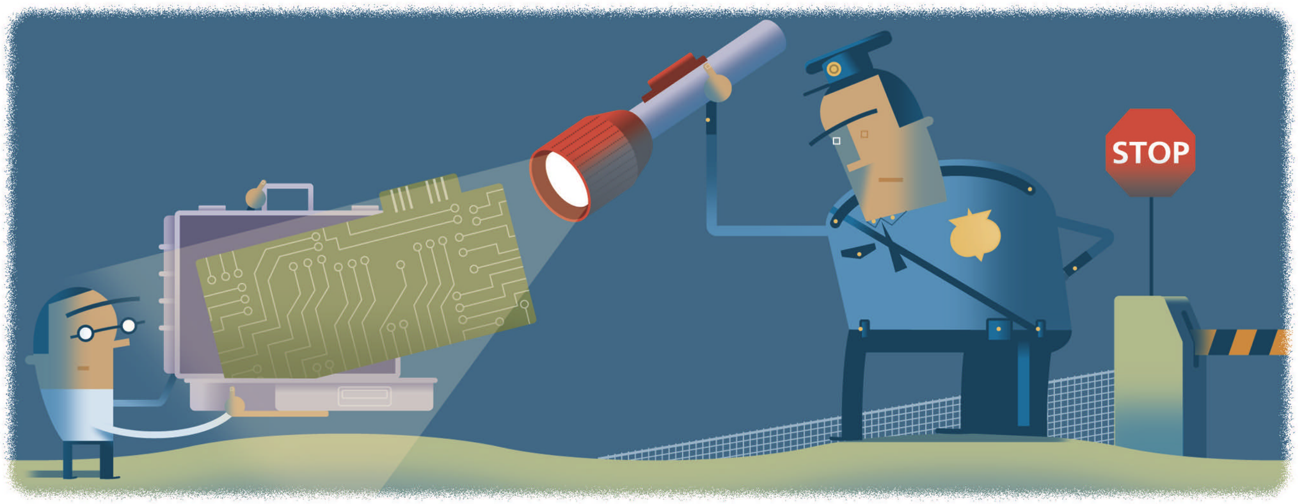
DANIEL VASCONCELLOS



DANIEL GUIDERA

BEYOND ROHS: THE GREENING OF GLOBAL MARKETS

BY MARGERY CONNER • TECHNICAL EDITOR

US AND ASIAN GOVERNMENTS ARE ABOUT TO IMPOSE THEIR OWN VERSIONS OF THE EU'S ROHS DIRECTIVE. RATHER THAN TARGETING EACH REGION'S REGULATIONS, MANUFACTURERS MAY STANDARDIZE ON THE MOST STRINGENT "GREEN" DIRECTIVE. THIS MOVE WILL AFFECT EVEN PRODUCTS THAT ARE EXEMPT FROM REGULATION, AS COMPONENT MANUFACTURERS MOVE AWAY FROM NONCOMPLIANT PARTS.

For the past three years, the electronics industry has been eyeing this month as the time that the European Union's ROHS (reduction-of-hazardous-substances) directive was supposed to take effect for some electronic products. Barring any last-minute legal maneuvers or postponements, electronic products bound for the multibillion-dollar European consumer market will need to satisfy the directive's limitations on six hazardous materials: lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers (**Reference 1**). The directive mandates that electronic products that do not comply with the directive's restrictions, calling for the elimination of these six substances, will face removal from the market and their manufacturers will have to pay fines.

Predictions of what will happen this month in Europe as the deadline passes run the gamut from business as usual with a smooth transition to a brave, new, lead-free world to major lawsuits halting the imposition of the directive. Some scenarios even predict a nightmare for European officials as they attempt to establish documentation requirements and enforce them on the fly. Regardless of the short-term outcome, the world of electronics will never go back to its "pregreen" state; rather, EU ROHS is just the first of many government-imposed regulations of environmental substances.

China passed its own version of ROHS in February, with an effective date of March 1, 2007 (**Reference 2**). The law specifies the same six substances as the European ROHS and then throws in a wild card: "other toxic or hazard substances or elements set by the State." China may not only regulate more substances but also allow a different amount of those substances. "'Lead-free' in the EU ROHS means it has less than 1000 ppm of lead in it," says Greg Roberts, marketing vice president of EMA, a value-added reseller of Cadence software. "Other countries selling products into China will

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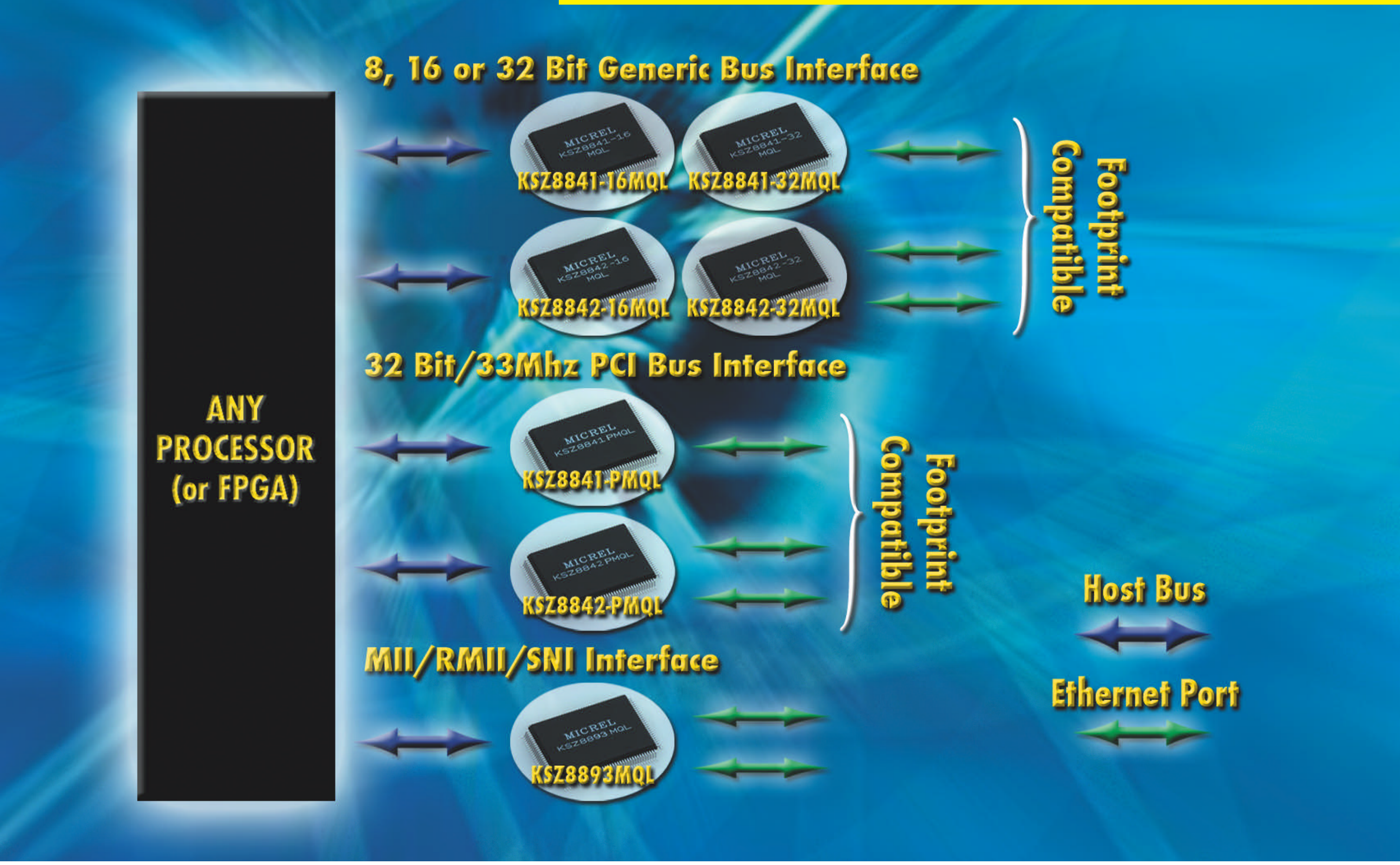

The road to network connectivity is never smooth but Micrel has you covered. Whether you need networking via an 8, 16 or 32-bit generic-bus, PCI-bus, MII, RMII, or SNI host interfaces, Micrel has the answer in easy to install single and dual-port Ethernet solutions. The devices address the growing need for streamlined networking connectivity in IP-Set Top Boxes, VoIP phones, Network Printers, Industrial Controls and networked Game Console applications, to name but a few. The dual port devices have the lowest latency (sub 310nS) in the industry and are ideal for daisy-chaining applications, or simply as two port switches to connect to voice, video and data.

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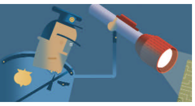

AT A GLANCE

- Expect China, Korea, Australia, and California to be among the first to implement "green" regulations.
- It's shortsighted to implement a documentation system that tracks only yes/no compliance for the European Union's ROHS (reduction-of-hazardous-substances) regulation.
- Ensure that your system can adapt to an increasingly regulated industry.
- Long leadtimes, higher prices, and accelerated end-of-life cycles will affect even manufacturers eligible for exemptions for lead parts as component manufacturers seek to standardize on green parts.

be subject to China's ROHS directive, which may have a lower allowable lead content. A product that could be lead-free or ROHS-compliant for Europe may not be compliant in China." (For some suggestions on how to make your designs globally compliant, see **sidebar** "Seven tips for the brave new world of 'green' regulations.")

The EU has not yet spelled out what kind of a documentation system it expects or what is sufficient for a manufacturer to prove it and its suppliers are in full compliance. It will determine what constitutes adequate documentation during these early months of the ROHS implementation, with companies involved in early test cases serving as guinea pigs. However, China's ROHS apparently will be more hands-on, with companies possibly having to prove their compliance upfront by undergoing testing at labs in China.

Some manufacturers currently track their EU ROHS parts' compliance with a simple spreadsheet listing each part and a yes/no check box under ROHS compliance. Is this enough documentation to satisfy the EU's directive? "It is until somebody challenges you," says EMA's Roberts. "The directive says you have 30 days to compile all the documentation on every component in your product line, including the traceability of the information. It requires materials declaration for everything in your product all the way down to the resistors, including the box it's in and the labels on it."

The OEM that the product packing lists is liable for compliance for the entire system. For example, if you purchase a power supply for your design and the manufacturer claims that it complies with the directive, you as the system manufacturer are still responsible for the liability of that entire assembly. "Many component vendors just give you a certificate and say 'yes, we're compliant,'" says Keith Hopwood, vice president of marketing for Phihong USA. "I say, 'show me.'"

A simple yes/no spreadsheet probably will not survive an EU ROHS challenge, and it has the additional drawback of being unable to adapt as regions impose different regulations. A robust system will go beyond yes/no EU ROHS compliance and track the actual parts-per-million count for all environmentally sensitive substances. However, it may be difficult to achieve that goal in the allotted time frame, cautions Eric Larkin, chief technology officer for Arena Solutions, a provider of Web-based PLM (product-life-cycle management). "If you believe that you're going to be able to get a full substance-level breakdown for every single component on your pc board within the 2006 to 2007 time frame, I don't see that happening," he says. "We know of only four component manufacturers that are looking at publishing the detailed substance-level breakdown."

A survey of customers by Toshiba's Discrete Products Division corroborates Larkin's view. "Lack of material content information is one of the biggest hurdles that many companies are facing right now," says Cynthia Pham, senior quality-assurance engineer for Toshiba.

MORE AT EDN.COM

- Visit www.edn.com/green to see ROHS (reduction-of-hazardous-substances)-compliance information from electronics manufacturers, distributors, and consulting organizations.
- Go to www.edn.com/060720df1 and click on Feedback Loop to post a comment on this article.

Despite the well-publicized ROHS deadline of July 1, 2006, regional preparedness varies widely. According to Jim Smith, senior vice president of warehouse and distribution worldwide at Avnet Logistics, EU countries' ROHS readiness is well ahead of the Americas', which in turn is ahead of the Asian countries. The reason that the EU is so far ahead is that the directive is the region's own regulation. Also, although European market share might account for only15% of US vendors' market share, it accounts for at least half for most European OEMs. A more subtle reason is that Europeans have seen a well-publicized example of the EU's will to enforce environmental regulations. In 2001, the Dutch government blocked the sales of 1.3 million Sony PlayStations in the EU because the systems' cables violated an EU environmental directive limiting the amount of cadmium (**Reference 3**). The incident demonstrates that even large, well-known brands are subject to the regulations. Although Sony's supplier provided the noncompliant cables, Sony incurred the penalties and loss of revenue.

What can trigger an EU ROHS challenge? Companies that have incurred the expense and time of complying with EU ROHS use their compliance as a competitive advantage against less green competitors. They can file a claim, triggering an EU audit of another company's system. Compliant vendors see this whistle-blowing as a fair tactic against noncompliant competitors.

Another reason that Asian manufacturers may lag behind in ROHS compliance is that they are waiting to see what China's ROHS initiative comprises. China's directive may not be significantly stricter than the EU ROHS because one of China's strengths is its competitive market pricing, and the Chinese government may be loath to put that advantage at risk. Regardless of China's eventual stance, you can expect the industry standard to evolve from the regulations of those regions with significant markets and that impose the strictest regulations.

Component manufacturers cannot justify multiple production lines for parts with the same functions. This reluctance or inability to make both green and nongreen versions has important implications

for companies that assume that the EU ROHS doesn't affect them—either because they don't sell into the EU market or because they have an exemption. Expect to see longer leadtimes, part shortages, and rising prices for noncompliant parts; ultimately, manufacturers will consign these parts to end-of-life status.

For example, medical and military devices are exempt from EU ROHS compliance and can continue to use leaded solder. "Defense vendors might have a problem before too long, because, once a supplier consigns a part to end-of-life status, raises the price, or extends the leadtime, that has huge ramifications in the supply chain," says Avnet's Smith. "If I'm the manufacturer of a part, I have to decide: If I can't make money doing both, which do I eliminate?" As EMA's Roberts points out, "The supply chain is the real driver in industry, not legislation."

ROHS has a companion directive, WEEE (waste electrical and electronics equipment), which specifies the marking of electrical and electronic products to facilitate their recycling. Again, deter-

SEVEN TIPS FOR THE BRAVE NEW WORLD OF "GREEN" REGULATIONS

• You can't rely on contract manufacturers to manufacture your products to ROHS (reduction-of-hazardous-substances) specifications. "Your contract manufacturer won't go to court for you," says Greg Roberts, marketing vice president of EMA, a value-added reseller of Cadence software.

• Even if you're exempt, you may still have a supply-chain problem. Suppliers will move inexorably to lead-free manufacturing, and other customers will bid up the price of any lead parts vital to their designs.

• You cannot mix and match lead and lead-free parts. According to electronic-component distributor Newark InOne, you can't assume backward compatibility with green, lead-free parts (Reference A).

• Manufacturers will gradually remove lead parts from the supply chain, making those parts obsolete. Roberts estimates that it will take four to five years for the supply chain to stabilize; until then, parts availability will remain in flux.

• The ROHS directives cover more than electronics. You should also pay attention to the mechanical assembly and parts, such as cadmium-plated screws.

• Know what market you are selling your design into, suggests Eric Larkin, chief technology officer for Arena Solutions, a provider of Web-based PLM (product-life-cycle management). This constraint is a new one for design engineers, who have traditionally had little interest in the geographical regions in which their products would sell. If your design is targeting the Chinese market, understand how or whether China's regulations differ from the European Union's ROHS directive.

• Ensure that your vendors assign part numbers to green parts different from those that they assigned to the older, "non-green" parts. Lack of part-number distinction is one of the top concerns in a recent ROHS-customer survey by Toshiba's Discrete Products Division. "All of Toshiba's lead-free products have a different part number to distinguish the lead-free and non-lead-free versions," says Cynthia Pham, senior quality-assurance engineer for Toshiba. "Not every company is doing this. It's a logistics nightmare if you use parts without unique numbers," she says (Figure A).

REFERENCE

A Shafer, Jeff, "ROHS compliant doesn't necessarily mean backwards compatible," www.newarkinone.com/services/rohs/backward_compatible.html.

Figure A Toshiba's original green product markings say "lead-free" (left), but customers want them to say "ROHS-compatible" or "ROHS-compliant." Toshiba maintains that only completed systems can be ROHS-compliant and marks its products that do not contain restricted substances "ROHS-compatible" (right).

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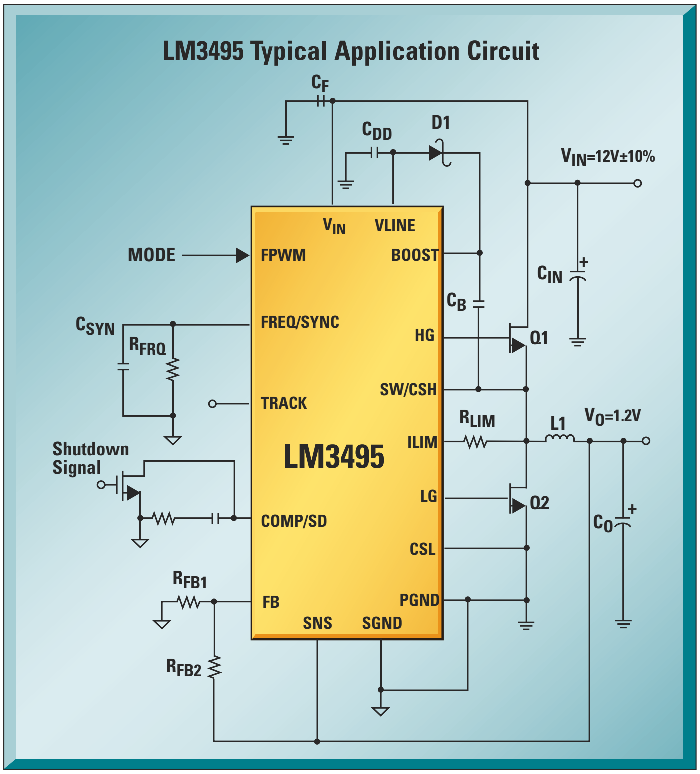

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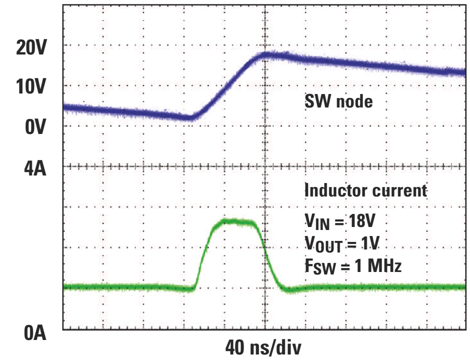

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mining how to make disposal and recycling more efficient goes beyond EU countries: Japan has had such a regulation, the HARL (Home Appliances Recycling Law), in place since 2001, and California is moving toward a similar law, with other states likely to follow. HARL and WEEE both require manufacturers to be responsible for accepting and recycling their products. However, the Japanese law allows for the consumer to pay a separate fee for recycling, whereas WEEE requires that the regional price of the equipment include the fee. This new additional cost to the manufacturer will drive designers to allow for the most effective means of recycling their products. Phihong USA's Hopgood gives an example the company encountered: "Under WEEE, if capacitors are over a certain size, they have to be removed from the board before recycling," he says. "Designers will want to avoid using parts that trigger recycling exceptions, if possible."

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ROHS is not an anomaly. Arena Solution's Larkin gives this perspective: "Go back to Upton Sinclair's *The Jungle* 100 years ago. When he wrote his novel about the Chicago slaughterhouses, the public became aware that there was a compelling public interest in regulating the quality and preparation of food and medicine. That realization led to the creation of the Food and Drug Administration and the regulatory environment under which both the food and medical industry work today." Just as today, we take for granted that modern producers provide food and medicine with regulations and laws, so too, will electronic-equipment manufacturing evolve into a regulated process. And the best, most efficient product designs will be ready and able to adapt to these regulations.EDN

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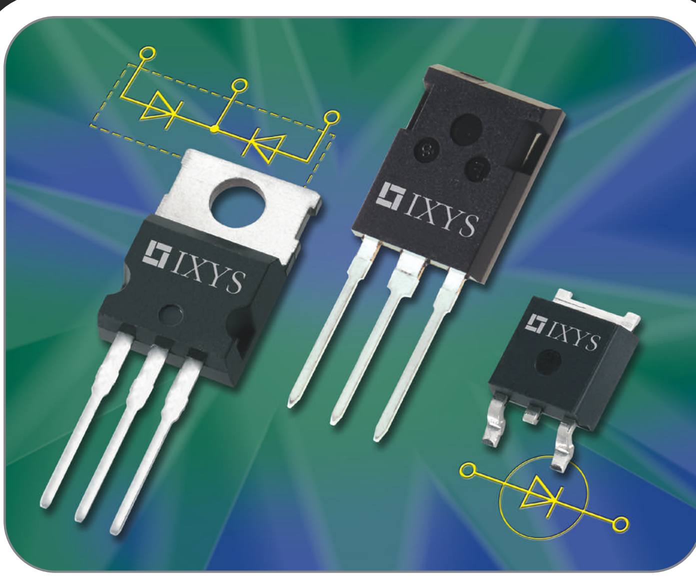

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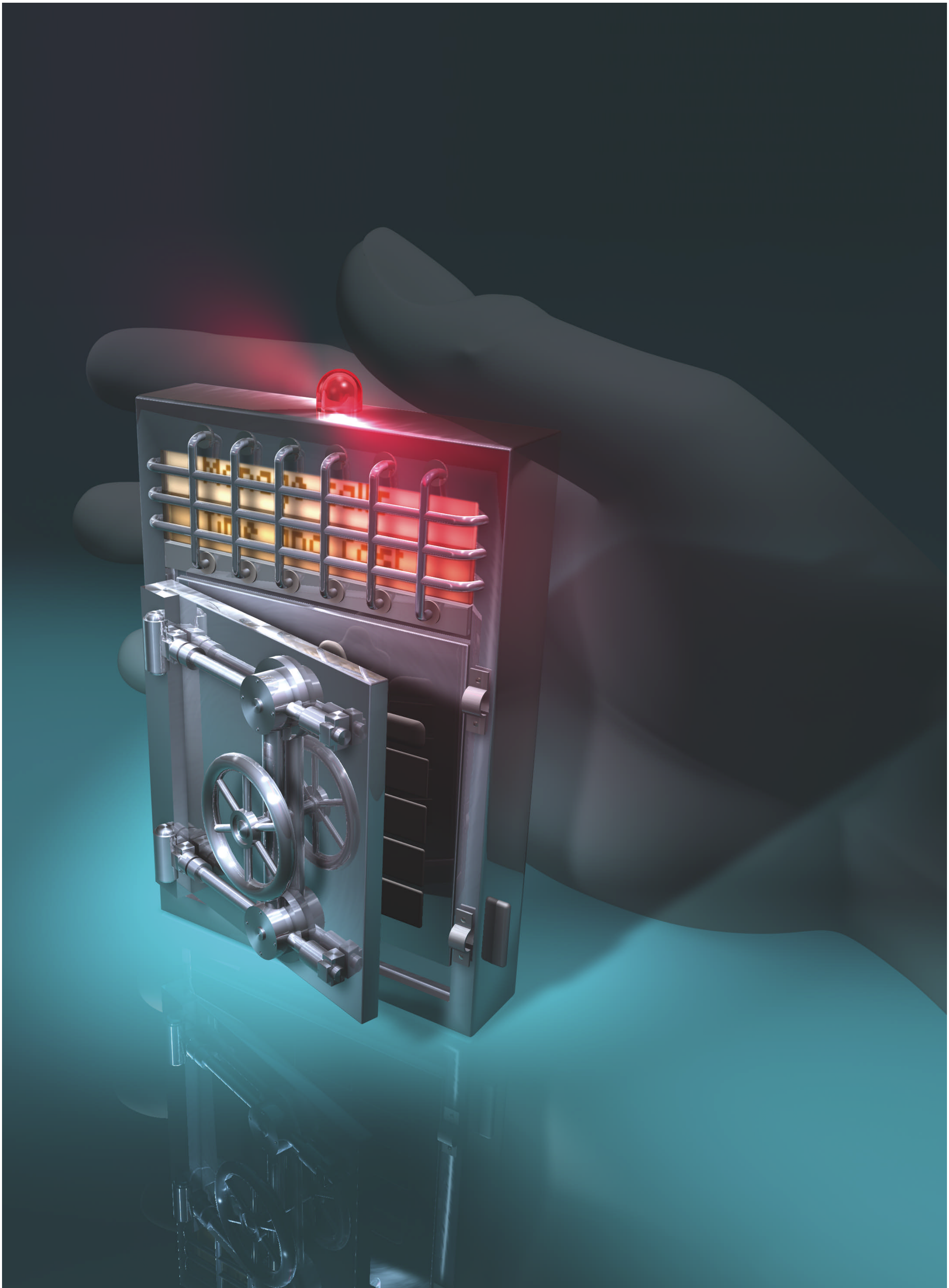


HACK-PROOF DESIGN

SECURITY REQUIREMENTS NOW TOP THE EMBEDDED-SYSTEM DESIGNER'S CHECKLIST AS NETWORKED DEVICES MULTIPLY AND HACKERS OPTIMIZE THEIR ATTACK TECHNIQUES.

BY WARREN WEBB • TECHNICAL EDITOR

As embedded devices permeate society and assume ever more important roles, the consequences of security failures are potentially catastrophic. Embedded devices provide unattended operation for thousands of mission-critical or safety-related systems in sectors such as manufacturing, health care, transportation, finance, and the military. Although we rely on these embedded systems without giving them a second thought, any one could be the potential target of casual hackers, organized crime, terrorists, or even adversary governments. The responsibility to protect against these attacks falls squarely on the shoulders of the system designer, who must secure not only the data that passes through or is stored on his embedded device, but also the intellectual property of the product itself.

Historically, designers physically protected and isolated embedded devices to achieve reasonable data security. Today, widespread interconnectivity may expose a critical embedded system to data extraction or process manipulation from anywhere in the world.

Unlike desktop systems, an embedded product must incorporate all security measures before its deployment. Embedded-system designers cannot wait for a breach and then devise a patch to cover security flaws. Users expect embedded products to perform a function for years without modification, and you can't stop or reboot many devices without risking loss of life, property, or critical information.

Security must be a prime design consideration from conception through production, deployment, and end-of-life disposal, because it is almost impossible to add to products currently in the field. The NIST (National Institute of Standards and Technology) provides designers with a number of security-related publications at its CSRC (Computer Security Resource Center). These documents outline life-cycle design principles to consider, such as security-policy definition, product design, threat identification, technological options, and programmer education. For example, the first challenge is to identify what data or proprietary information requires protection before selecting safeguards. It may be possible to reduce or even eliminate sensitive data to minimize the security effort. Next, you should

AT A GLANCE

- Threats to portable devices force designers to include physical packaging protection in addition to traditional software safeguards.
- Unlike the desktop-software practice of patch after failure, embedded products must continue operation in spite of security threats.
- Widely available cryptography algorithms and secure protocols offer embedded-system designers the best security protection for Internet-connected devices.
- New pay-as-you-go business models rely on secure hardware and software architectures to allow customers to pay for pricey systems as they use them.

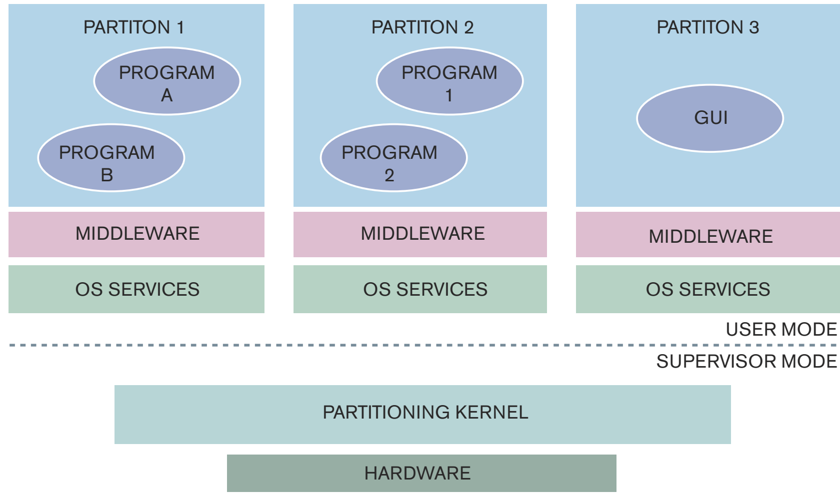


Figure 1 The MILS (Multiple Independent Levels of Security) architecture isolates kernel, middleware, and application components (courtesy LynuxWorks).

determine your possible attackers and their level of sophistication. A simple password may stop a curious amateur, but determined intruders require multiple levels of security.

SEPARATE AND SECURE

An obvious security measure is to physically isolate networked systems from outside influence. If you can collocate the embedded system and server on the same network segment without Internet access, most security problems disappear. Isolation is especially effective in highly critical applications, such as controlling a factory, where disruption would be costly. Minimizing the connection time to the Internet can also thwart many hacking attempts. A short-term connection to exchange data at random times prevents search robots from identifying your system. However, if your embedded system is a target of a hacker, short connections will only delay unauthorized access.

Attackers can steal embedded devices, especially portable products, disassemble them, and probe them with sensitive test equipment to extract data. They can remove memory elements from the products to possibly extract their contents. Likewise, they can use active debugging ports and software to read sensitive data or force unintended operation. Attackers may even monitor electromagnetic radiation or force the system to operate outside its design parameters, with extreme temperatures, voltage excursions, and clock variations, to gain information.

Equipment designers should also incorporate physical deterrents to safeguard sensitive or proprietary information. A hardened enclosure requiring specialized equipment to open may deter some attacks. Internally, designers should engineer pc boards with security in mind. For example, BGA packages with critical signals hidden on internal board layers complicate probing and reverse-engineering. Although you can remove some formulations with acid, epoxies and conformal coatings also provide protection to all or part of a

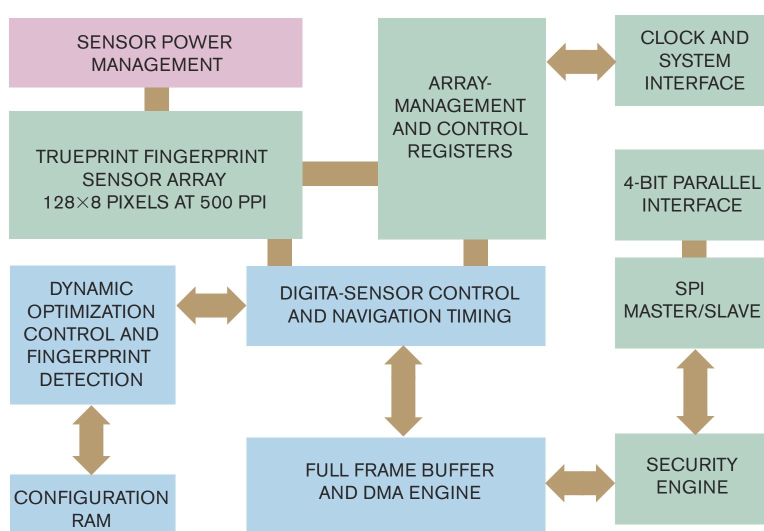


Figure 2 With a 12×5-mm footprint, the EntréPad 1510 slide sensor from AuthenTec enables secure fingerprint authentication on portable devices.

product's sensitive internal circuitry.

To establish standards for system security, the United States, Canada, and several European nations created the "Common Criteria for Information Technology Security Evaluation" usually referred to as "the Common Criteria." The Common Criteria Web site includes a developer section with guidelines and complete documentation. The Common Criteria structure allows consumers, developers, and evaluators to specify the security functions of a product in standard-protection profiles and EALs (evaluation-assurance levels). Another embedded-

SAFEGUARDING KEYS

By Kris Ardis, Dallas Semiconductor/Maxim

When most people think about security, they first think of encryption. An embedded system that sends and receives only triple-DES (Data Encrypted Standard)-encrypted commands might seem difficult to crack. However, imagine a house that has the most advanced door locks and an electronic security system; it would also be difficult to crack. An enterprising thief would not try to circumvent the house's protection but instead would attempt to steal the keys or coerce the security code from the homeowner. Embedded systems are prone to the same weakness: All the encryption in the world is futile if someone steals the encryption key.

Proper key protection starts with where you store the keys. The safest place is in the same place you will use them. Embedded systems, therefore, need to store encryption keys inside a microcontroller and never allow the keys to leave. If you store the key in an external memory, such as a serial EEPROM or an external RAM, the microcontroller would need to fetch the key before using it. When the external memory transmits the key to the microcontroller, it transmits it in the clear, allowing anyone with an oscilloscope or a logic analyzer to discover the key data.

On-chip EEPROM or flash may also be inadequate protection. A determined attacker could remove the microcontroller's plastic packaging and use a microprobe to inspect the memory cells. In high-security applications, losing the key would be catastrophic. An attacker would have unimpeded access to financial networks or could create undetectable fake-ID cards.

High-security applications present unique challenges for IC designers. Secure microcontrollers, such as Dallas Semiconductor's DS5250, address this design challenge by providing battery-backed, nonvolatile SRAM for on-chip key storage. This custom-designed memory can link to several tamper-detection circuits, both on- and off-chip, and instantly erase when the situation meets one of several tampering criteria. Some on-chip sensors, such as temperature and voltage detectors, respond to fault-injection attacks. Such attacks occur when the secure microcontroller is operating outside its maximum operating range, attempting to make cryptographic operations fail so that the device leaks key data. Another kind of on-chip sensor detects microprobing attacks. A silicon mesh in the top layer of the chip initiates a "tamper destruct" if someone shorts or breaks its submicron traces. Secure microcontrollers also include self-destruct input pins that external mechanisms, such as microswitches, light sensors, and pressure sensors, can trigger.

Although physical protection of the key is critical, so is logical protection. Secure microcontrollers offer encryption accelerators that can quickly and securely execute standard algorithms. Public-key operations such as RSA (Rivest, Shamir, and Adleman) execute in milliseconds, and symmetric algorithms such as triple DES run in microseconds. Hardware accelerators are more resistant to timing attacks than software algorithms, because they complete in the same number of machine cycles regardless of the actual values of the keys or the data. Secure microcontrollers also incorporate hardware random-number generators that vary in behavior over voltage, temperature, and process variations, making it impossible for an attacker to guess the value of generated keys or blinding values.

Encrypted program memories provide further logical protection for the applications running on secure microcontrollers. When you first initialize the system, the secure microcontroller uses the on-chip random-number generator to create a unique key, which the system uses to encrypt the program space. When the device executes, the system decrypts the encrypted instructions and places them in an on-chip cache in real time. This method not only protects intellectual property and thwarts reverse-engineering, but also prevents an attacker from executing malicious code.

Applications concerned with security have unique challenges to meet. By designing secure microcontrollers with physical and logical security in mind, you can create the safest foundation for applications that must protect secret keys.

AUTHOR'S BIOGRAPHY

Kris Ardis is a product manager for secure microcontrollers at Dallas Semiconductor/Maxim.

software security standard, MILS (Multiple Independent Levels of Security), requires a partitioned real-time operating system that you can certify with rigorous tests (**Figure 1**). Memory protection and guaranteed resource availability allow you to manage secure and nonsecure data on a single processor. The MILS architecture allows designers to create application code with tamperproof security features that you cannot bypass, that you can verify mathematically, and that the system always invokes.

Before a user can interact with a secure embedded system, he must undergo an authentication process to verify his identity. Authentication scenarios may include combinations of a secret password; a physiological trait, such as a fingerprint; or a security device, such as a smart card or key. For example, the Entré-Pad 1510 slide sensor from AuthenTec enables fingerprint authentication for portable devices such as cell phones. Contained in a 12×5-mm, 40-pin BGA package, the sensor includes a dense 128×8-pixel-detection matrix along with pattern-matching firmware (**Figure 2**). Hackers have been successful in obtaining passwords by visually or electronically capturing keystrokes or simply asking for them through a variety of subterfuges. Often, passwords pass over local wired or wireless networks in the clear or unencrypted, and attackers can capture them with simple packet-capture programs widely available on the Internet.

CODE AND DECODE

When an embedded system must connect to a network or the Internet, designers turn to encryption to safeguard their data. Effective encryption schemes work equally well over wired, wireless, or power-line communications systems. Two basic types of encryption algorithms are in use today, both relying on a secret key plus an encoding sequence to transform plain text into cipher text and vice versa. With symmetric encryption, the sender and receiver use the same key to encrypt and decipher a message. Asymmetric encryption uses two keys—one for encryption and another for decryption. Public-key cryptography is a popular form of asymmetric encryption that makes one of the keys available publicly and keeps

Figure 3 The Spartan P630 targets military-manpack applications with a hardened, sealed enclosure and software for preboot access control and data encryption.

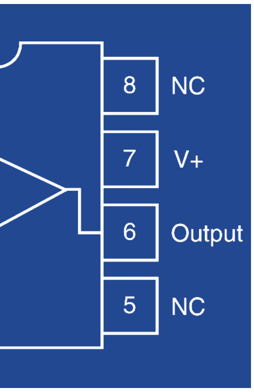
the other secret. Key distribution and secrecy are fundamental problems in cryptographic security systems (see **sidebar** "Safeguarding keys").

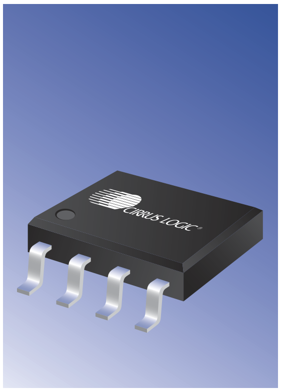
The most widely used security protocol for TCP/IP network traffic is the SSL (Secure Sockets Layer), which provides data encryption, server authentication, message integrity, and optional client authentication. SSL comes in 128- and 256-bit versions whose names refer to the length of the session key that encrypted transactions generate. The longer the key, the more secure the encrypted data. IPSec (Internet Protocol Security), another

Figure 4 Security features allow Pure Digital to profitably offer customers a one-time-use video camcorder for less than $40.

encryption standard, implements security at the network layer and allows the system to transparently encrypt network traffic. You can install IPSec in a gateway computer to secure all traffic passing onto the Internet without adding overhead to individual network nodes. Like most other security protocols, IPSec includes provisions for both key and message exchange. Virtual private networks use IPSec to create secure networks over the Internet.

Targeting military-manpack applications in which security is paramount, General Micro Systems recently introduced a secure portable PC with a 6.5×3×0.5-in. main-board footprint (**Figure 3**). The Spartan P630 is a hardened PC featuring a 1.4-GHz Pentium-M processor, as much as 2 Mbytes of L2 cache, an embedded GPS (global-positioning-system) receiver, and 802.11b/g wireless communications in a pocket-sized form factor. The company can configure the device with as much as 2 Gbytes of ECC memory, 16 Gbytes of bootable flash, as much as 60 Gbytes of hard-disk drive, and an LCD/touchscreen in a hardened, sealed enclosure. To ensure secure operation, Spartan includes software for preboot access control and data encryption along with automatic file deletion if someone compromises the system. Spartan also features a six-hour bat-





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The CS3013 and CS3014 also feature low power consumption—approximately 50 percent lower compared to competing ICs—which is important for new generations of battery-powered portable instruments and personal monitoring applications.

With these new products, Cirrus Logic has strengthened its portfolio of high-precision analog ICs for applications demanding superior high-resolution measurement.

tery life and is available in a conduction-cooled version operating at −40 to +85°C or a standard convection-cooled version with a 0 to 55°C temperature range. Packaging options include a titanium-aluminum enclosure for rugged applications. Software support for the P630 is available under Windows XP, Linux, QNX, and VxWorks. Prices for the conduction-cooled version start at $3400 (100).

SECURE BUSINESS

With improving security, device manufacturers are experimenting with business models to attract more customers. In the pay-as-you-go scenario, customers receive a fully functional device and promise to pay for it as they use it or over the life of a subscription plan. If the customer fails to make a payment, the vendor can disable the device by withholding network-activation codes. A strong security model then prevents the customer from bypassing activation or removing parts.

For example, Microsoft recently announced FlexGo, a pay-as-you-go platform to extend PC ownership into emerging markets. FlexGo requires that system components individually track usage based on active minutes or a specific end date. When a consumer has used all of the available computer time, Microsoft limits access to the PC until the consumer adds more time. The company also imposes usage limitations when there are signs of system tampering. Microsoft has also added secure operating-system components to enable metered use of the software. A FlexGo software-development kit allows businesses to use their own billing systems to manage Microsoft's provisioning system to offer pay-as-you-go computer-use time to customers.

With stand-alone embedded-security challenges, Pure Digital manufactures a pocket-sized, one-time-use camcorder that records as much as 20 minutes of video and audio (**Figure 4**). The device is available through several camera- and convenience-store outlets for as little as $20 plus a $12 processing charge to copy your movies onto a DVD. The device includes a fixed-focus lens, a 1.4-in. color LCD, and speaker plus operator controls to record, play back, and delete unwanted scenes. Although the device is a hacker's delight, and several Web sites are devoted to extracting the video without returning the camcorder for processing, there are sufficient security measures to deter most users.

Security precautions and potential information-disclosure consequences have changed the fundamental design goals for embedded products. Designers are no longer driven to produce the simplest, lowest cost device for each project. Security requirements have forced designers to beef up resources with faster, more capable processors, secure data storage, and tamperproof hardware to protect the system and data while executing the application. EDN

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For more on a one-time-use video-camera, go to www.edn.com/article/CA629314.

For some history on embedded-device security, go to www.edn.com/article/CA434871.

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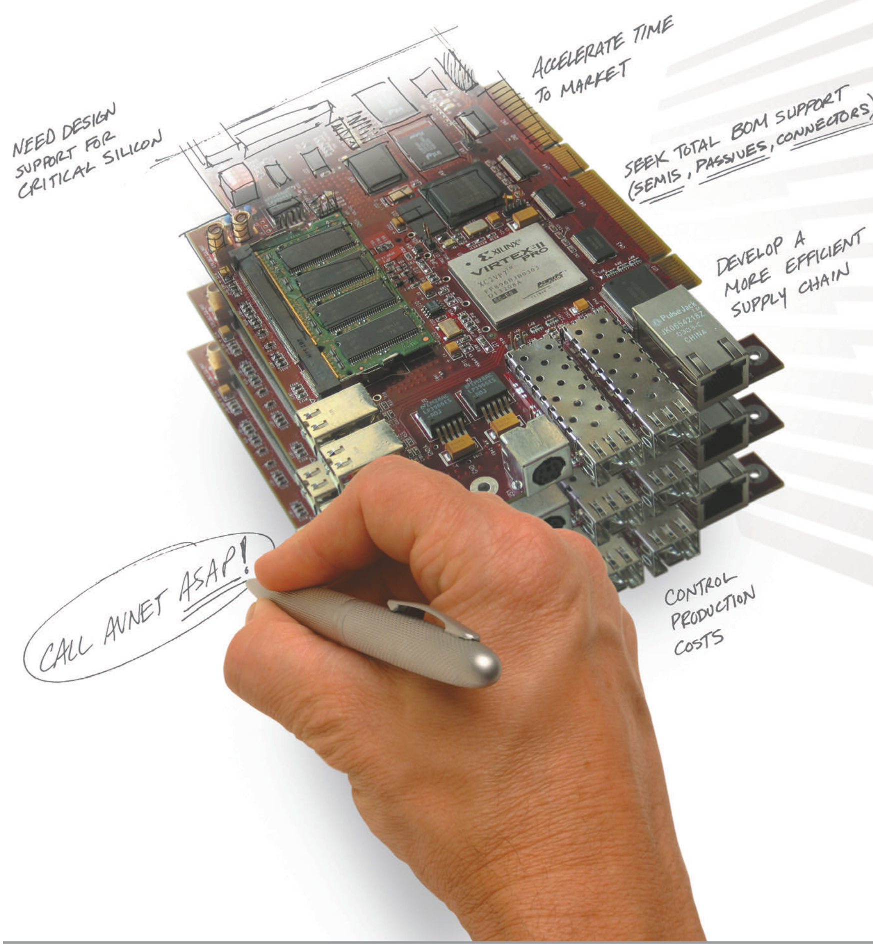

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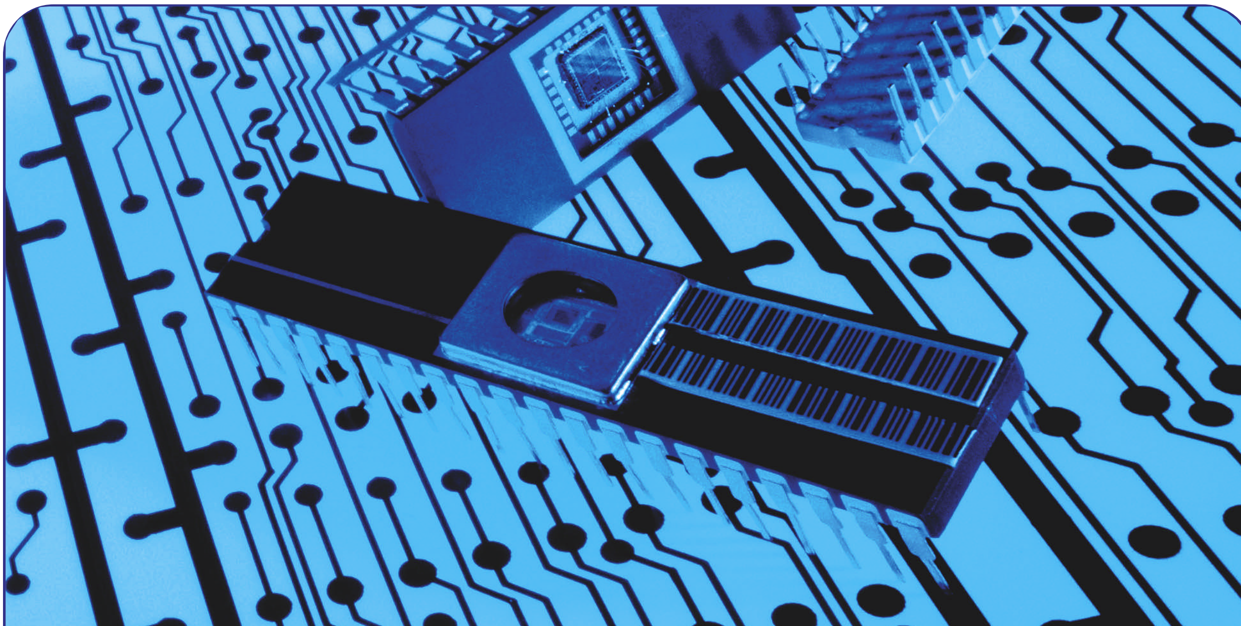


Typical Field Programmable Gate Array Power Requirements

The flexibility of FPGAs leads to the requirement for multiple supply voltages and currents.

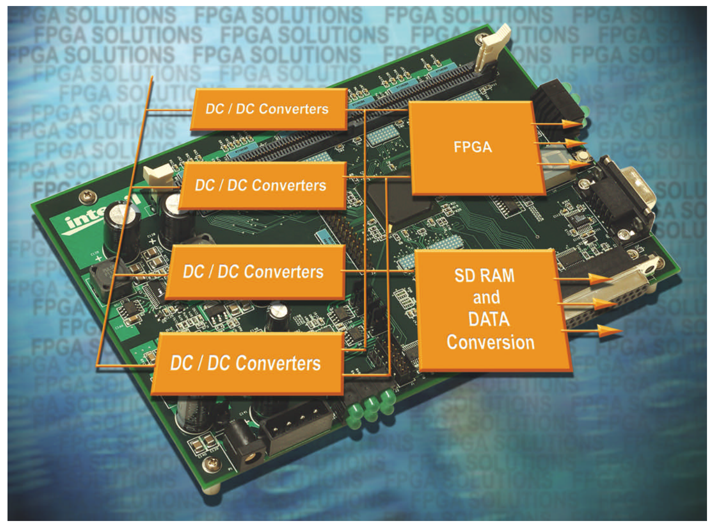
Core Voltage / Power

In large FPGAs, the logic core generally has the most demanding current requirements, up to tens of amps depending on the number of gates being used and the clock frequency. Designated V_{CCINT} by Altera, by platform the voltage required is:

- Stratix® and Cyclone® series = 1.5V
- Stratix II series = 1.2V

I/O Voltage / Power

Designated V_{CCO} and equal to 1.5V, 1.8V, 2.5V or 3.3V depending on the I/O standard selected. I/O standards can be set independently by block in the FPGA, so more than one I/O voltage for a single FPGA is possible.



Intersil's Power Management Portfolio of DC/DC Regulators, PWM and LDO Controllers

3.3V Input	V_{IN} (V)		I_{OUT} (max)(A)	# of Outputs	Int. FET	V_{OUT} (V)		Device Description	Package
	Min	Max				Min	Max		
ISL6410	3	3.6	0.6	1	Y	1.2	1.8	0.6 Amp PWM Regulator with Selectable V_{OUT} of 1.8, 1.5, or 1.2V, f_{sw} 750kHz, Adj POR delay in QFN pkg.	10 MSOP, 16 QFN
ISL6455	3	3.6	0.6	3	Y	0.8	2.5	0.6 Amp PWM Regulator and Dual 0.3 Amp LDOs and Reset	24 QFN
ISL8011	2.5	5.5	1	1	Y	0.8	V_{IN}	1.2 Amp PWM Regulator, f_{sw} 1.4MHz	10 DFN
EL7532	2.5	5.5	2	1	Y	0.8	V_{IN}	2 Amp PWM Regulator with 100mS Power On Reset, f_{sw} 1.5MHz	10 MSOP
ISL8012*	2.7	5.5	2	1	Y	0.8	V_{IN}	2 Amp PWM Regulator with pre-biased load start-up, f_{sw} 1.5MHz	14 HTSSOP, 14 QFN
ISL8013	2.5	5.5	3	1	Y	0.8	V_{IN}	3 Amp PWM Regulator with 100mS Power On Reset	14 HTSSOP
ISL8014*	2.7	5.5	4	1	Y	0.8	V_{IN}	4 Amp PWM Regulator with pre-biased load start-up, f_{sw} 1.5MHz	14 HTSSOP, 14 QFN
EL7554	3	6	4	1	Y	0.8	V_{IN}	4 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
EL7566	3	6	6	1	Y	0.8	V_{IN}	6 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
ISL65424	2.375	5.5	4	2	Y	0.6	V_{IN}	Dual 4A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL65426	2.375	5.5	6	2	Y	0.6	V_{IN}	Dual 6A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL6406	3	3.6	20	1		0.8	0.95 x V_{IN}	PWM Controller with Adj f_{sw} 100kHz to 770kHz with Ext Freq Sync	16 SOIC, 16 TSSOP, 16 QFN
ISL6439	3	3.6	20	1		0.8	V_{IN}	PWM Controller with f_{sw} 300 or 600kHz	14 SOIC, 16 QFN
ISL6527/A	3	3.6	20	1		0.8	V_{IN}	PWM Controller with f_{sw} 300 or 600kHz, External Reference	14 SOIC, 16 QFN
ISL8104	1.2	12	20	1		0.6	V_{IN}	PWM Controller with 50kHz to 1.5MHz f_{sw}	14 SOIC
ISL8105/A	1	12	20	1		0.6	V_{IN}	PWM Controller with 300kHz and 600kHz options	14 SOIC

* Coming Soon

5V Input	V_{IN} (V)		I_{OUT} (max)(A)	# of Outputs	Int. FET	V_{OUT} (V)		Device Description	Package
	Min	Max				Min	Max		
ISL6410A	4.5	5.5	0.6	1	Y	1.2	3.3	0.6 Amp PWM Regulator with Selectable V_{OUT} of 3.3, 1.8, or 1.2V, f_{sw} 750kHz, Adj POR delay in QFN pkg.	10 MSOP, 16 QFN
ISL6455A	4.5	5.5	0.6	3	Y	0.8	3.3	0.6 Amp PWM Regulator and Dual 0.3 Amp LDOs and Reset	24 QFN
ISL8011	2.5	5.5	1	1	Y	0.8	V_{IN}	1.2 Amp PWM Regulator, f_{sw} 1.4MHz	10 DFN
EL7532	2.5	5.5	2	1	Y	0.8	V_{IN}	2 Amp PWM Regulator with 100mS Power On Reset, f_{sw} 1.5MHz	10 MSOP
ISL8012*	2.7	5.5	2	1	Y	0.8	V_{IN}	2 Amp PWM Regulator with pre-biased load start-up, f_{sw} 1.5MHz	14 HTSSOP, 14 QFN
ISL8013	2.5	5.5	3	1	Y	0.8	V_{IN}	3 Amp PWM Regulator with 100mS Power On Reset	14 HTSSOP
ISL8014*	2.7	5.5	4	1	Y	0.8	V_{IN}	4 Amp PWM Regulator with pre-biased load start-up, f_{sw} 1.5MHz	14 HTSSOP, 14 QFN
EL7554	3	6	4	1	Y	0.8	V_{IN}	4 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
EL7566	3	6	6	1	Y	0.8	V_{IN}	6 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
ISL8502*	4.5	5.5	2	1	Y	0.6	V_{IN}	2 Amp PWM Regulator with Integrated MOSFETs	24 QFN
ISL8501*	4.5	5.5	1	1	Y	0.6	V_{IN}	1 Amp PWM Regulator with Dual 0.45 Amp LDOs	24 QFN
ISL65424	2.375	5.5	4	2	Y	0.6	V_{IN}	Dual 4A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL65426	2.375	5.5	6	2	Y	0.6	V_{IN}	Dual 6A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL6440	4.5	5.5	10	2		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz	24 QSOP
ISL6445	4.5	5.5	10	2		0.8	5.5	Dual Synchronous Buck PWM Controller with Wide V_{IN}, f_{sw} 1.4MHz	24 QSOP
ISL6441	4.5	5.5	6	3		0.8	0.7 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 1.4MHz and Linear Controller	28 QFN
ISL6442	4.5	5.5	20	3		0.8	V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 2.4MHz and Linear Controller	24 QSOP
ISL6443	4.5	5.5	10	3		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz and Linear Controller	28 QFN
ISL6420A	4.5	5.5	20	1		0.6	V_{IN}	PWM Controller with Wide V_{IN}, Start-Up into Pre-Bias Load	20 QFN, 20 QSOP
ISL6406	4.5	5.5	20	1		0.8	0.95 x V_{IN}	PWM Controller with Adj f_{sw} 100kHz to 770kHz with Ext Freq Sync	16 SOIC, 16 TSSOP, 16 QFN
ISL6439	4.5	5.5	20	1		0.8	V_{IN}	PWM Controller with 300 or 600kHz Osc	14 SOIC, 16 QFN
ISL6527/A	4.5	5.5	20	1		0.8	V_{IN}	PWM Controller with 300 or 600kHz Osc, External Reference	14 SOIC, 16 QFN
ISL6521	4.5	5.5	20	4		0.8	4.5	PWM Controller and Triple Linear Controllers	16 SOIC
ISL8104	1.2	12	20	1		0.6	V_{IN}	PWM Controller with 50kHz to 1.5mHz f_{sw}	14 SOIC, 14 QFN
ISL8105/A	1	12	20	1		0.6	V_{IN}	PWM Controller with 300kHz and 600kHz options	14 SOIC, 14 QFN
ISL8101	5	12	≥60	1		0.6	2.3	Two Phase Multiphase Buck PWM Controller with MOSFET Drivers, f_{sw} 250kHz/Phase	24 QFN
ISL8102	5	12	80	1		0.6	2.3	Two Phase Buck PWM Controller with High Current MOSFET Drivers, f_{sw} 1.5MHz/Phase	32 QFN
ISL8103	5	12	100	1		0.6	2.3	Three Phase Buck PWM Controller with High Current MOSFET Drivers, f_{sw} 1.5MHz/Phase	40 QFN

12V Input	V_{IN} (V)		I_{OUT} (max)(A)	# of Outputs	Int. FET	V_{OUT} (V)		Device Description	Package
	Min	Max				Min	Max		
ISL8502*	5.6	15	2	1	Y	0.6	V_{IN}	2 Amp PWM Regulator with Integrated MOSFETs	24 QFN
ISL8501*	5.6	22	1	3	Y	0.6	V_{IN}	1 Amp PWM Regulator with Dual 0.45 Amp LDOs	24 QFN
ISL6440	5.6	24	10	2		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz	24 QSOP
ISL6445	5.6	24	10	2		0.8	5.5	Dual Synchronous Buck PWM Controller with Wide V_{IN}, f_{sw} 1.4MHz	24 QSOP
ISL6441	5.6	24	6	3		0.8	0.7 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 1.4MHz and Linear Controller	28 QFN
ISL6442	5.6	24	20	3		0.8	V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 2.4MHz and Linear Controller	24 QSOP
ISL6443	5.6	24	10	3		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz and Linear Controller	28 QFN
ISL6420A	5.6	28	20	1		0.6	V_{IN}	PWM Controller with Wide V_{IN}, Start-Up into Pre-Bias Load	20 QFN, 20 QSOP
ISL8104	1.2	12	20	1		0.6	V_{IN}	PWM Controller with 50kHz to 1.5MHz f_{sw}	14 SOIC
ISL8105/A	1	12	20	1		0.6	V_{IN}	PWM Controller with 300kHz and 600kHz options	14 SOIC
ISL8101	5	12	≥60	1		0.6	2.3	Two Phase Multiphase Buck PWM Controller with MOSFET Drivers, f_{sw} 250kHz/Phase	24 QFN
ISL8102	5	12	80	1		0.6	2.3	Two Phase Buck PWM Controller with High Current MOSFET Drivers, f_{sw} 1.5MHz/Phase	32 QFN
ISL8103	5	12	100	1		0.6	2.3	Three Phase Buck PWM Controller with High Current MOSFET Drivers, f_{sw} 1.5MHz/Phase	40 QFN

* Coming Soon

The “One-Chip” Power Solution

Intersil’s multi-output family of PWM controllers and Integrated FET regulators support up to four rails, providing a “one-chip” solution for most applications.

Multiple Output/Multi-Phase IFETs and Controllers

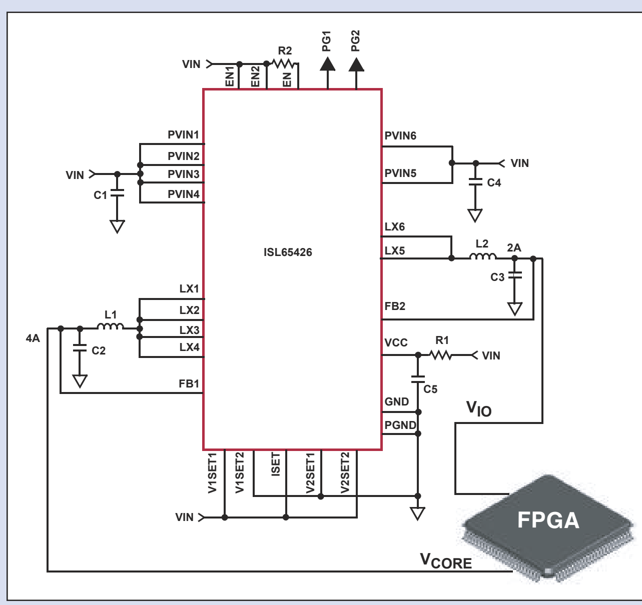
Part Number	Architecture	Input Voltage Range (V)	Output Voltage Range (V)	I_{OUT} max (A)
ISL6455	1 PWM Regulator + 2 LDOs	3.0-3.6	0.8-2.5	0.6
ISL6455A	1 PWM Regulator + 2 LDOs	4.5-5.5	0.8-3.3	0.6
ISL8501	1 PWM Regulator + 2 LDOs	6.0-22	0.6-22	1
ISL6440	2 PWMs	4.5-24	0.8-24	10
ISL6445	2 PWMs	4.5-24	0.8-5.5	10
ISL6441	2 PWMs (f_{sw} = 1.4MHz) + Linear Controller	4.5-24	0.8-24	20
ISL6442	2 PWMs (f_{sw} = 2.5MHz) + Linear Controller	4.5-24	0.8-24	20
ISL6443	2 PWMs (f_{sw} = 300kHz) + Linear Controller	4.5-24	0.8-24	20
ISL65424	2 PWM Regulators	2.375-5.5	0.6-5.5	4
ISL65426	2 PWM Regulators	2.375-5.5	0.6-5.5	6
ISL8101	3 Phase PWM	5.0-12	0.6-2.3	100
ISL8102	2 Phase PWM	5.0-12	0.6-2.3	60
ISL8103	2 Phase PWM	5.0-12	0.8375-1.6	60-80

ISL65426: 6A Dual Synchronous Regulators for V_{CCINT} and V_{CCO}

The ISL65426 is a high efficiency dual output synchronous buck regulator with integrated power MOSFETs, tailor-made for FPGA power solutions. Operating from an input bias ranging from 2.375V to 5.5V, the single ship solution provides two output voltages which are selectable or externally adjustable from 0.8V to 4.0V while delivering up to 6A of total output current. The two regulator outputs can be used to supply V_{CCINT} and V_{CCIO} with a reduced number of external components and high efficiency.

The power block contains six 1A capable blocks to support one of the four output configuration options (3A:3A, 4A:2A, 5A:1A, 2A:4A).

High integration contained in a thin Quad Flat No-Lead (QFN) package makes the ISL65426 the ideal choice to power small form factor power management applications.



I1SET	I2SET	IOUT1	CHANNEL1 CONNECTIONS	IOUT2	CHANNEL2 CONNECTIONS
1	1	3A	LX1, LX2, LX3	3A	LX4, LX5, LX6
1	0	4A	LX1, LX2, LX3, LX4	2A	LX5, LX6
0	1	5A	LX1, LX2, LX3, LX4, LX6	1A	LX5
0	0	2A	LX1, LX2	4A	LX3, LX4, LX5, LX6

ISL6521: PWM Controllers for V_{CCINT} and Linear Regulators for V_{CCO1}, V_{CCAUX}, and V_{CCO2}

Combination products that incorporate multiple switchers and/or linears in a single package are an excellent choice for many FPGA-based designs. These combination devices can provide all the voltages required from a single IC or board, and they can be adjusted to provide the optimum responses for the end application. Good layout and bypassing techniques plus excellent on-chip isolation prevents the supplies from interacting.

The ISL6521 can provide the required currents and voltages for the latest generation of Altera FPGAs (for example Stratix II, Stratix and Cyclone series) in a 16-pin SOIC package with minimal external components. The ISL6521 implements a highly efficient synchronous buck design and in addition includes three linear regulators, which can provide additional voltages to the board. I_{CCO} and I_{CCAUX} currents less than 120mA can be supplied directly from the linear regulator drive pins (as shown here for V_{CCO2}) or they can be used to control an external transistor (as shown here for V_{CCO1} and V_{CCAUX}).

The complete datasheet for the ISL6521 is available at www.intersil.com/data/fn/fn9148.pdf. Simulation tools are also available at www.intersil.com/isim/.

ISL644X: High Efficiency Dual, Step Down PWM Controllers with Single Linear Controller

300kHz to 2.5MHz Family of Dual, 180° Out-of-Phase, PWM Controllers + Linear Controller

The ISL644X family of controllers can create a highly efficient triple-output solution by using 180° out-of-phase synchronous buck switchers to supply V_{CCINT} and V_{CCIO}. It also has an internal 5V Linear regulator that can sink and source current. The Linear regulator can source up to 6A using an external transistor. The ISL644X family offers a wide input range of V_{IN} from 5.6V to 24V and 4.5V to 5.6V.

The two PWMs synchronized 180° out-of-phase reduce the RMS input current and ripple voltage, hence can supply both Core and I/O voltages independently. The ISL644X family incorporates several Protection and supervisory features. Power-up sequencing is available through the integrated programmable Soft-Start. The outputs can be adjustable down to 0.8V and up to 24V. The efficiency of the ISL644X family is enhanced by using the lower MOSFET $R_{DS(ON)}$.

The complete datasheet for the ISL6441 is available at www.intersil.com/data/fn/fn9197.pdf. Simulation tools are also available at www.intersil.com/isim/.

ISL6420A: Advanced Single Synchronous Buck PWM Controller

The ISL6420A is an excellent solution for all the FPGA family's power requirements. It has a wide input voltage range from 4.5V to 28V and a programmable output current capability up to 20A.

The core or the I/O voltages are supplied by a synchronous buck switcher with fast transient response which makes the solution very efficient. The output voltages of the ISL6420A are fully adjustable from 0.6V to 28V, with a maximum tolerance of ±1.0% over temperature and line voltage variations.

The switching frequency is resistor selectable from 100kHz to 1.4MHz which offers cost and space savings. The ISL6420A integrates control, output adjustment, monitoring and protection functions into a single package. The ISL6420A is available in QFN and QSOP packages.

The complete datasheet for the ISL6420A is available at www.intersil.com/data/fn/fn9169.pdf. Simulation tools are also available at www.intersil.com/isim/.

>20A Solutions: ISL8102 Multi-phase Buck PWM Controller

As the current requirements of the board rise to greater than 20A, more sophisticated power supply solutions are required to maintain well-regulated supply voltages. By distributing the power and load current, implementation of multi-phase converters utilize smaller and lower cost transistors with fewer passives. These reductions are possible due to the phase interleaving process of this topology.

The ISL8102 is a two-phase PWM control IC with Integrated MOSFET drivers. It has the system voltage regulation accuracy up to ±0.5% over temperature. It integrates an optional Load Line (Droop) programming, using the loss-less inductor DCR current sampling. Precision channel current sharing is implemented using loss-less $R_{DS(ON)}$ current sampling, which makes it a highly efficient solution.

The complete datasheet for the ISL8102 is available at www.intersil.com/data/fn/fn9247.pdf. Simulation tools are also available at www.intersil.com/isim/.

Stratix-II Power Requirement Summary

	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
V_{CCINT}	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
V_{CCIO}	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V
I_{CCINT} (max)	4A	6A	7A	9A	12A	16A
I_{CCIO} (max)	10A (all 8 banks)	10A (all 8 banks)	10A (all 8 banks)	10A (all 8 banks)	10A (all 8 banks)	10A (all 8 banks)

Intersil Power Solutions for Stratix-II FPGAs

		Input Supply			
		V_{IN} = 3.3V	V_{IN} = 5V	V_{IN} = 12V	V_{IN} = 24V
V_{CCINT}					
V_{CCINT} = 1.2V	$I_{CCINT} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCINT} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCINT} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCINT} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCINT} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	$I_{CCINT} \geq$ 10A	EL7554, EL7556, ISL6406	ISL6406, ISL6439, ISL6527/A	ISL6420A	ISL6420A
V_{CCIO}					
V_{CCIO} = 1.5V	$I_{CCIO} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	$I_{CCIO} \geq$ 10A	EL7554, EL7556, ISL6406	ISL6406, ISL6439, ISL6527/A	ISL6420A	ISL6420A
V_{CCIO} = 1.8V	$I_{CCIO} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	$I_{CCIO} \geq$ 10A	EL7554, EL7556, ISL6406	ISL6406, ISL6439, ISL6527/A	ISL6420A	ISL6420A
V_{CCIO} = 2.5V	$I_{CCIO} \leq$ 600mA	ISL8010	ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	$I_{CCIO} \geq$ 10A	EL7554, EL7556, ISL6406	ISL6406, ISL6439, ISL6527/A	ISL6420A	ISL6420A
V_{CCIO} = 3.3V	$I_{CCIO} \leq$ 600mA	ISL8010, ISL6410A	ISL8010, ISL6410A	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	$I_{CCIO} \geq$ 10A	EL7554, EL7556, ISL6406, ISL8104, ISL8105A	ISL6406, ISL6439, ISL6527/A, ISL8104, ISL8105A	ISL6420A, ISL8104, ISL8105A	ISL6420A
V_{CCPD}					
V_{CCPD} = 3.3V	$I_{CCPD} \leq$ 300mA	ISL8010, ISL6410A	ISL8501, ISL8502	ISL6420A	ISL6420A

* Coming Soon

Stratix Power Requirement Summary

	EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80
V_{CCINT}	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V
V_{CCIO}	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V
I_{CCINT} (max)	1.5A	3.5A	4A	5.5A	6A	7.5A	10A
I_{CCIO} (max)	12A (all 8 banks)	12A (all 8 banks)	12A (all 8 banks)	12A (all 8 banks)	12A (all 8 banks)	12A (all 8 banks)	12A (all 8 banks)

Intersil Power Solutions for Stratix FPGAs

		Input Supply			
		V_{IN} = 3.3V	V_{IN} = 5V	V_{IN} = 12V	V_{IN} = 24V
V_{CCINT}					
V_{CCINT} = 1.5V	I_{CCINT} ≤ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCINT} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCINT} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCINT} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCINT} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	I_{CCINT} ≥ 10A	EL7554, EL7556, ISL6406	ISL6406, ISL6439, ISL6527/A	ISL6420A	ISL6420A
V_{CCIO}					
V_{CCIO} = 1.5V	I_{CCIO} ≤ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	I_{CCIO} ≥ 10A	EL7554, EL7556, ISL6406, ISL8104, ISL8105A	ISL6406, ISL6439, ISL6527/A, ISL8104, ISL8105A	ISL6420A, ISL8104, ISL8105A	ISL6420A
V_{CCIO} = 1.8V	I_{CCIO} ≤ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	I_{CCIO} ≥ 10A	EL7554, EL7556, ISL6406, ISL8104, ISL8105A	ISL6406, ISL6439, ISL6527/A, ISL8104, ISL8105A	ISL6420A, ISL8104, ISL8105A	ISL6420A
V_{CCIO} = 2.5V	I_{CCIO} ≤ 600mA	ISL8010	ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	I_{CCIO} ≥ 10A	EL7554, EL7556, ISL6406, ISL8104, ISL8105A	ISL6406, ISL6439, ISL6527/A, ISL8104, ISL8105A	ISL6420A, ISL8104, ISL8105A	ISL6420A
V_{CCIO} = 3.3V	I_{CCIO} ≤ 600mA	ISL8010, ISL6410A	ISL8010, ISL6410A	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
	I_{CCIO} ≥ 10A	EL7554, EL7556, ISL6406, ISL8104, ISL8105A	ISL6406, ISL6439, ISL6527/A, ISL8104, ISL8105A	ISL6420A, ISL8104, ISL8105A	ISL6420A

* Coming Soon

Cyclone Power Requirement Summary

	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
V_{CCINT}	1.5V	1.5V	1.5V	1.5V	1.5V
V_{CCIO}	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V
I_{CCINT} (max)	750mA	1A	1.5A	3A	5A
I_{CCIO} (max)	6A (all 4 banks)	6A (all 4 banks)	6A (all 4 banks)	6A (all 4 banks)	6A (all 4 banks)

Intersil Power Solutions for Cyclone FPGAs

		Input Supply			
		V_{IN} = 3.3V	V_{IN} = 5V	V_{IN} = 12V	V_{IN} = 24V
V_{CCINT}					
V_{CCINT} = 1.5V	$I_{CCINT} \leq$ 600mA	ISL6410, EL7530	ISL6410A, EL7530	ISL8502, ISL8501	ISL6420A
	I_{CCINT} = 1A	ISL8011, EL7536	ISL8011, EL7536, ISL8501	ISL6420A	ISL6420A
	I_{CCINT} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCINT} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCINT} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
V_{CCIO}					
V_{CCIO} = 1.5V	$I_{CCIO} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
V_{CCIO} = 1.8V	$I_{CCIO} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
V_{CCIO} = 2.5V	$I_{CCIO} \leq$ 600mA	ISL8010	ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A
V_{CCIO} = 3.3V	$I_{CCIO} \leq$ 600mA	ISL8010, ISL6410A	ISL8010, ISL6410A	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
	I_{CCIO} = 2A	EL7532, ISL8012*	EL7532, ISL8012*	ISL6420A	ISL6420A
	I_{CCIO} = 3A	ISL8013	ISL8013	ISL6420A	ISL6420A
	I_{CCIO} = 4A-6A	EL7554, EL7556, ISL8014*	EL7554, EL7556, ISL8014*	ISL6420A	ISL6420A

* Coming Soon

MAX II Power Requirement Summary

	EPM240	EPM240G	EPM570	EPM570G	EPM1270	EPM1270G	EPM2210	EPM2210G
V_{CCINT}	2.5 or 3.3V	1.8V	2.5 or 3.3V	1.8V	2.5 or 3.3V	1.8V	2.5 or 3.3V	1.8V
V_{CCIO}	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V	1.5, 1.8, 2.5, 3.3V
I_{CCINT} (max)	75mA	75mA	125mA	125mA	250mA	250mA	400mA	400mA
I_{CCIO} (max)	450mA (both banks)	450mA (both banks)	450mA (both banks)	450mA (both banks)	900mA (all 4 banks)	900mA (all 4 banks)	900mA (all 4 banks)	900mA (all 4 banks)

Intersil Power Solutions for MAX-II CPLDs

		Input Supply			
		V_{IN} = 3.3V	V_{IN} = 5V	V_{IN} = 12V	V_{IN} = 24V
V_{CCINT}					
V_{CCINT} = 1.8V	$I_{CCINT} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCINT} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
V_{CCINT} = 2.5V	$I_{CCINT} \leq$ 600mA	ISL8010	ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCINT} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
V_{CCINT} = 3.3V	$I_{CCINT} \leq$ 600mA	ISL8010, ISL6410A	ISL8010, ISL6410A	ISL8502, ISL8501	ISL6420A
	I_{CCINT} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
V_{CCIO}					
V_{CCIO} = 1.5V	$I_{CCIO} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
V_{CCIO} = 1.8V	$I_{CCIO} \leq$ 600mA	ISL6410, ISL8010	ISL6410A, ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
V_{CCIO} = 2.5V	$I_{CCIO} \leq$ 600mA	ISL8010	ISL8010	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A
V_{CCIO} = 3.3V	$I_{CCIO} \leq$ 600mA	ISL8010, ISL6410A	ISL8010, ISL6410A	ISL8502, ISL8501	ISL6420A
	I_{CCIO} = 1A	ISL8011	ISL8011, ISL8501	ISL6420A	ISL6420A

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BY WILLIAM J. BOWHERS • MERRIMACK COLLEGE

Magnetic-field measurements hold the key to reducing dc/dc EMI

POWER CONVERTERS FREE SYSTEM DESIGNERS FROM UNWIELDY CONSTRAINTS, BUT THE DEVICES RADIATE UNSPECIFIED FIELDS THAT CAN DESTROY THE SIGNAL/NOISE PERFORMANCE OF SENSITIVE CIRCUITS NEARBY. MAGNETIC-FIELD MEASUREMENTS HOLD THE KEY TO FINDING AND CORRECTING THESE PROBLEMS.

Performance-driven measurement instrumentation requires low-noise, high-bandwidth linear front-end circuits that combine with equally well-performing A/D converters and clocking (**Figure 1**). Designers work to quantize the measurement of interest into a digital signal early in the processing chain to keep out unwanted noise. Look at your favorite instrumentation Web sites. A brief scan of dc-measurement and ac-source-and-measurement instrumentation turns up instruments with dynamic ranges of 120 dB or more. Engineering for dynamic range is a search for the source of every spurious signal. High-performance-instrument designers must be aware of all of the potential noise sources—not just the usual culprits, such as power supplies and digital activity. As dynamic range exceeds 100 dB, engineering for high SNR leads to investigating the charge pump running in the FPGA, the thermal gradient that occurs when the processor starts and stops, and the magnetic coupling from the other instrument that someone set on top of your instrument. A significant part of the design is isolating precision analog circuits from internal and external electromagnetic activity.

Today's instrumentation-and-measurement industry is undergoing a transformation. After years of performance-based engineering, market forces are leading to new open architectures (**Figure 2**). With customers wanting the advantages of open architecture without performance compromise, the new environment brings new engineering challenges.

For example, consider the semiconductor-test industry, in which the test requirements of SOC (system-

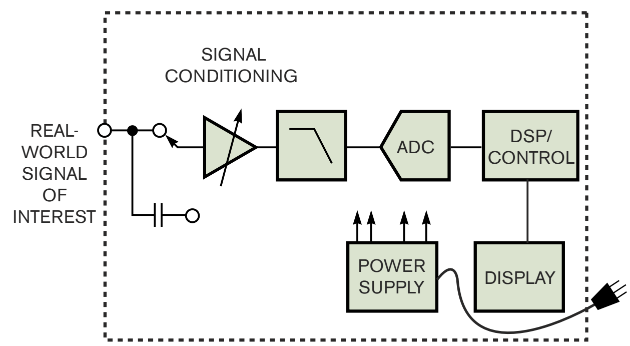


Figure 1 Performance-driven measurement instrumentation requires low-noise, high-bandwidth linear front-end circuits coupled to equivalent-performing A/D converters and clocking. It also requires a power supply, sometimes line-powered, as shown, but often a dc/dc converter.

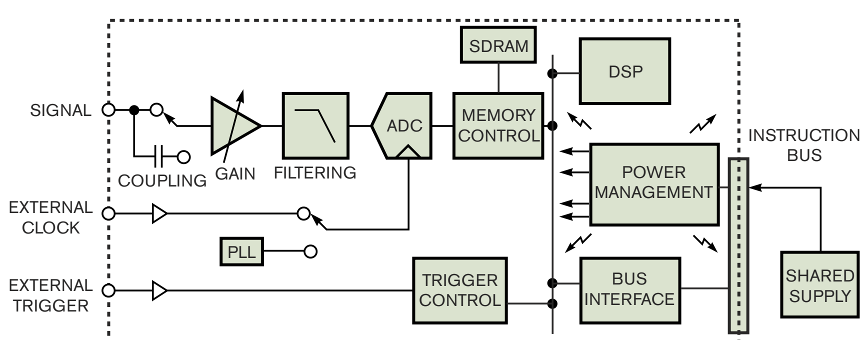


Figure 2 After years of performance-based engineering, market forces are leading to new open architectures. At the block-diagram level, open and proprietary architectures are similar, but, at the implementation level, the differences can be significant.

on-chip) ICs drive up the breadth of instrumentation that test systems must contain. Time to market and the cost of ownership of large ATE (automatic-test-equipment) systems have combined to define a critical need for an open-test-system architecture (**Reference 1**). The trend exceeds the bounds of just ATE, however. A growing need exists for high-performance, modular VXI and PXI instrumentation for production testing and characterization. Test-equipment architectures are opening up as a strategy to reduce cost through greater flexibility, which leads to higher efficiency, greater reuse, and lower barriers to competition among suppliers.

So where does this trend leave instrument-development teams? During the era of performance-driven design, development teams had control over a large part of the system architecture. That's not the case in open, card-modular architectures, such as VXI. In such architectures, the backplane interface and physical-packaging limits highly constrain design engineers. Engineers need to place more emphasis on environmental issues, such as cooling, power conversion, and EMI (electromagnetic interference). One of the more significant of these challenges is EMI from power-conversion components within the instrumentation system. A dc/dc converter within the system relieves a combination of space and power-supply constraints, but it also generates noise, which could be the factor that limits your spurious-free dynamic range. This scenario can occur whether this

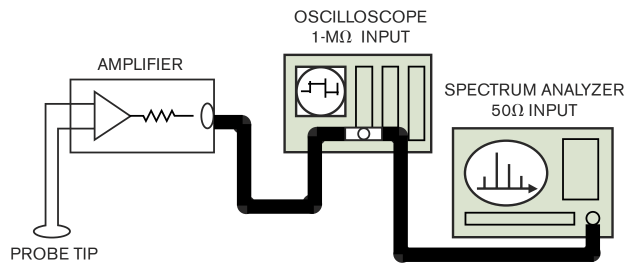


Figure 4 A wideband amplifier amplifies the pickup-loop output and drives an oscilloscope and a spectrum analyzer. Wiring the signal to the amplifier and from the amplifier to the instruments requires care to avoid introducing spurious signals that can reduce the measurement accuracy.

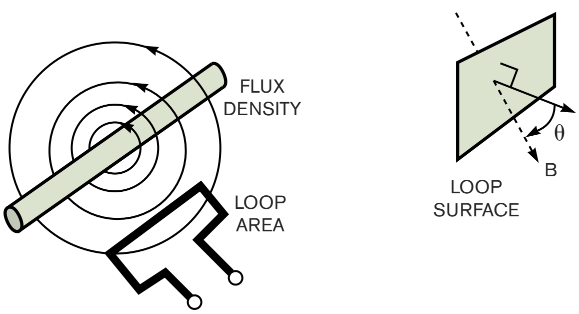


Figure 3 A varying magnetic field induces in a pickup loop a voltage proportional to the loop area and rate of change of the field component normal to the plane of the loop.

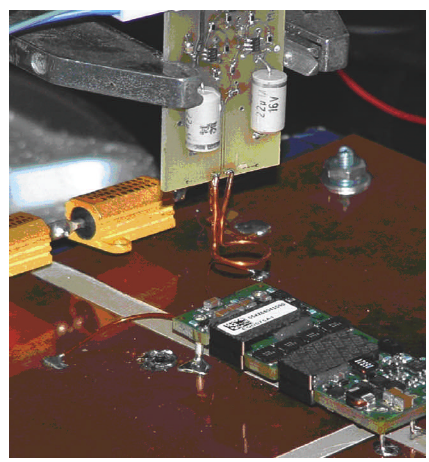


Figure 5 The intent is to place the pickup loop 1 in. above the plane that would represent the surface of the motherboard if the converter were mounted in an appropriate through-hole design.

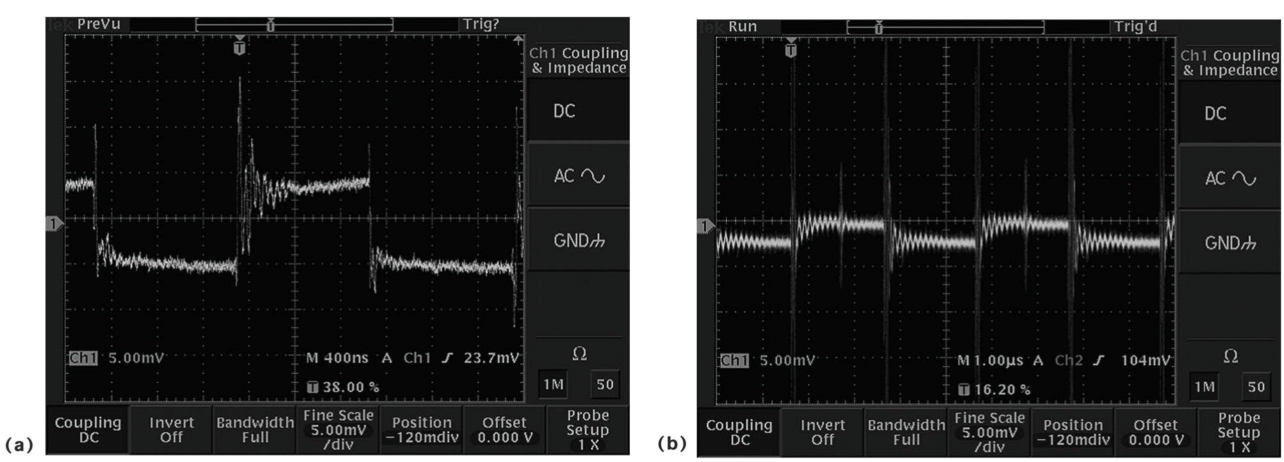
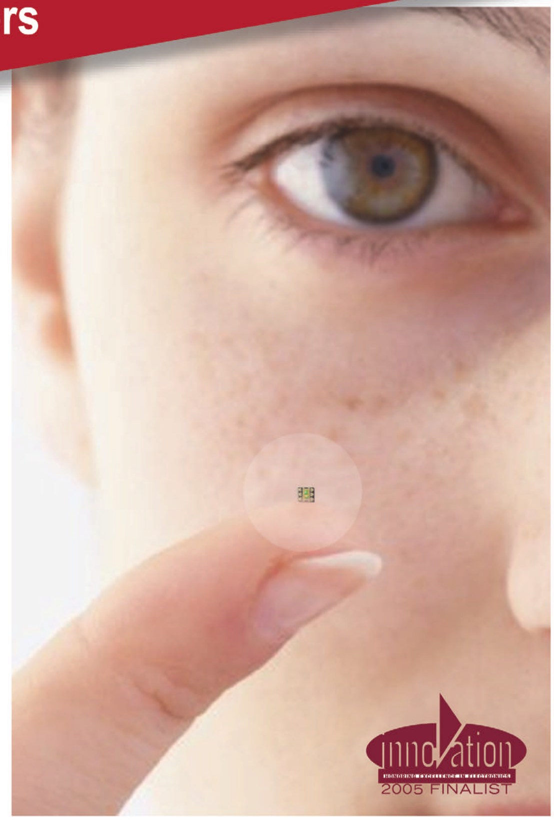


Figure 6 Although the two tested dc/dc converters, Brand X (a) and Brand Y (b), are equal in size, have the same basic architecture, and have nearly identical published specifications, the magnetic fields above them differ considerably.

Intersil Ambient Light Sensors

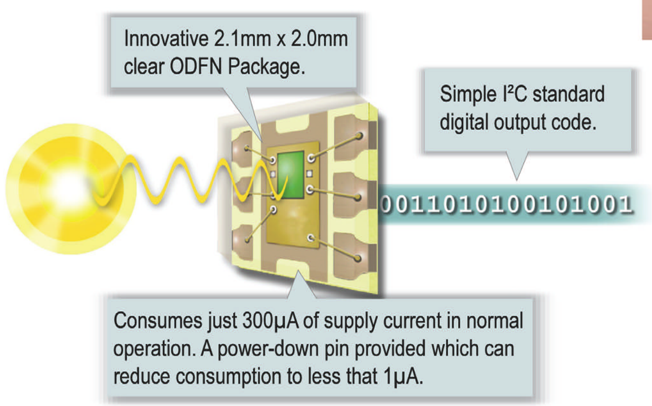
High Performance Analog

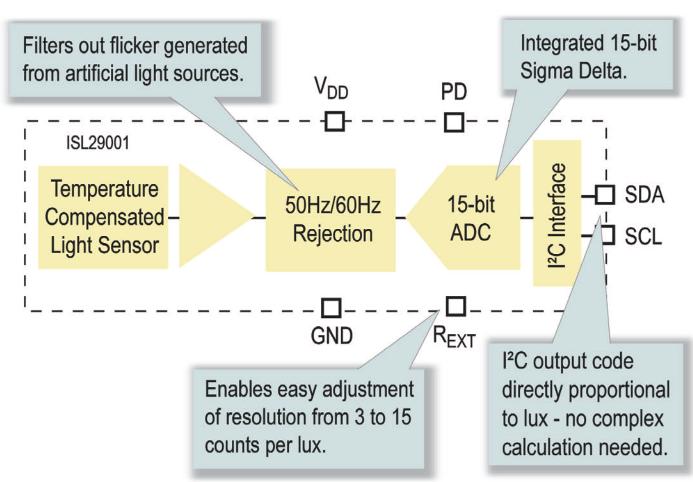
The Best Ambient Light Sensors and Their Closest Competitor



With light sensitivity only matched by the human eye, Intersil's ISL29001 Light-to-Digital Converter provides simple, pure 15-bit I²C digital data.

Drawing less than 300µA of supply current, the ISL29001 provides 15-bit effective resolution. This state-of-the art device integrates two photodiodes and an ADC into a super small 2.1mm x 2.0mm ODFN package. The digital data in standard I²C format couldn't be simpler to use. It's no wonder **EDN Magazine** has selected one of this family's light sensors as a finalist for this year's **Innovation of the Year Award**.





ISL29001 Key Features:

- I²C Interface produces simple I²C output code, directly proportional to lux
- 0.3 lux to 10,000 lux range
- 50Hz/60Hz rejection to eliminate artificial light flicker
- Human eye response
- 15-bit effective resolution
- Adjustable resolution: 3 to 15 counts per lux
- 2.5V to 3.3V supply
- Temperature compensated
- 6-pin ODFN (2.1mm x 2mm)
- Pb-Free plus anneal available (RoHS compliant)

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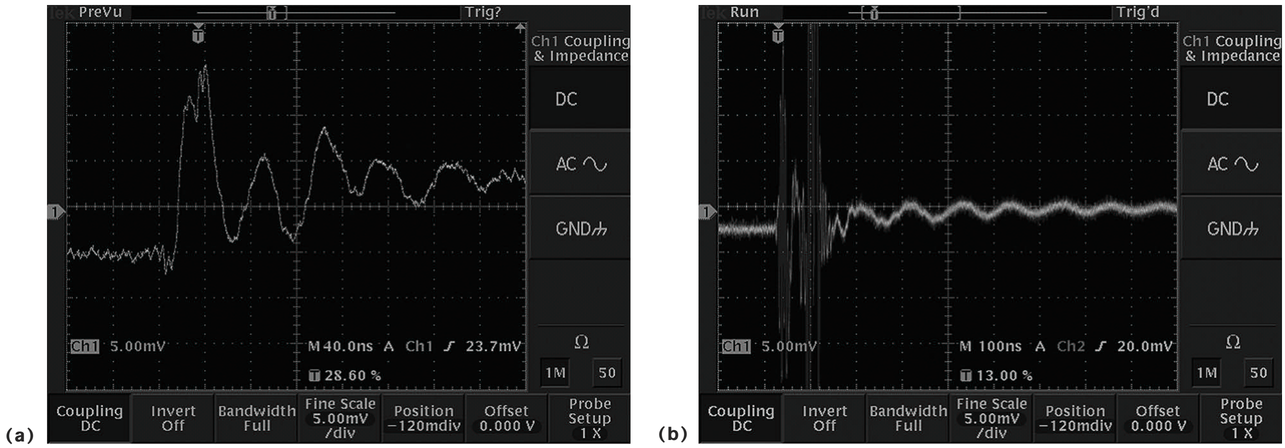


Figure 7 Whereas both converters, Brand X (a) and Brand Y (b), have similar switching characteristics, a faster sweep reveals that, although Brand Y's magnetizing inductance keeps emissions lower overall, the unit's leakage inductance resonates at a higher frequency and couples greater peak voltage at the switching transient.

TABLE 1 DATA FROM SAMPLES

Characteristic		Brand X	Brand Y
Switching frequency (kHz)		420	250
Time domain	Switching field (mV p-p)	9.5	2
	Switching field (µtesla p-p)	14.1	4.94
	Transient field (mV p-p)	20	160
	Transient field (tesla/sec)	24.7	197
Frequency domain	Fundamental field (dBm)	−36	−48
	Fundamental field (µtesla)	3.5	1.4
	Resonance (MHz)	20	9.1
	Resonant field (dBm)	−56	−55
	Resonant field (ntesla)	7	17.1

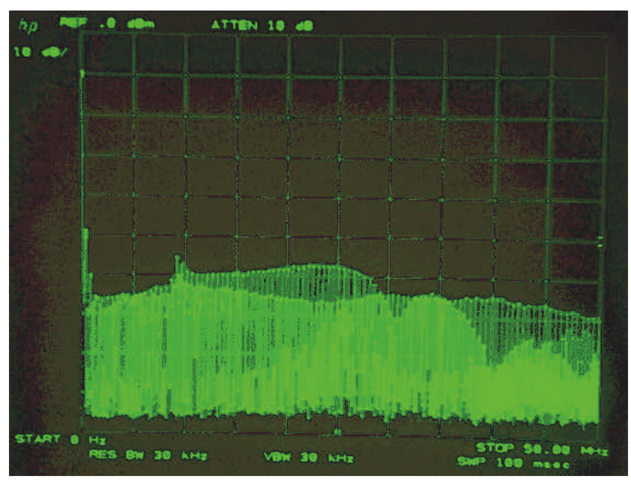


Figure 8 A broad look at the spectrum of Brand Y's field shows a resonance near 10 MHz with components peaking at 20 to 25 MHz.

noise originates in the affected instrument or from a noisy neighbor whose design did not require the same attention to dynamic-range requirements.

Instrumentation for an open architecture must comply with system specifications regardless of whether the instrument in the next slot is a highly dynamic power supply or a bank of 200-MHz digital-pin drivers. In this environment, every instrument must be tested to demonstrate compliance with a field-emission profile that imposes the same emission and susceptibility requirements on all instruments.

MAGNETIC COUPLING

Near-field, radiated EMI can create noise problems for sensitive instrumentation. Near fields contain both electric and magnetic fields in proportion to the impedance of the source (**Reference 2**). Low-impedance circuits—that is, low relative to the 377Ω impedance of free space, or air—emit predominantly magnetic fields, whereas high-impedance circuits emit predominantly electric fields. Coupling includes capacitive and mutually inductive coupling depending upon fields present and the configuration of the victim circuitry. Because circuit impedances in switch-mode power-supply circuits tend to be low and electric fields are relatively easy to shield, this article focuses on magnetic coupling **Figure 3**).

Faraday's Law leads to an understanding that the electromotive force—essentially voltage plus any resistive losses—in a circuit is proportional to the rate of change of the magnetic flux within the circuit. No voltage is induced if the rate of change is zero. Magnetic interference is an ac issue with a higher degree of coupling as frequency increases.

Magnetic flux, Φ_M, can be self-induced, as with the product of inductance and current, or mutually induced, as with the product of flux density and loop area (see **sidebar** "Magnetic circuits"). The relationship in the following **equation** is interesting: $E=-d\Phi_M/dt=d(LI)/dt=-d(BA\cos\theta)/dt$, where I is current, B is

(continued on pg 64)

MAKING YOUR OWN MAGNETIC-FIELD-MEASUREMENT PROBE

A high-bandwidth amplifier provides approximately 20 dB of gain to a signal that a small magnetic loop produces (Figure A). You can observe the probe output on a spectrum analyzer or an oscilloscope depending upon the application requirements. Many ac-source or -measurement instruments need to describe performance in terms of SFDR (spurious-free dynamic range) and would tend toward spectral data. However, dc instrumentation may be more concerned with total rms noise energy and would examine field measurements in the time domain. These component measurements look at both.

Figures B and C show the layout of the amplifier and probe tip. The probe tip provides a circular area with 0.4 in. diameter perpendicular to the circuitry on the pc board. An additional design consideration is to provide a balanced input to cancel any electric fields coupling to the probe tip.

This circuit uses high-bandwidth current-feedback op amps because the dc/dc converters that are most interesting for instrumentation development have resonant components of 25 to 60 MHz.

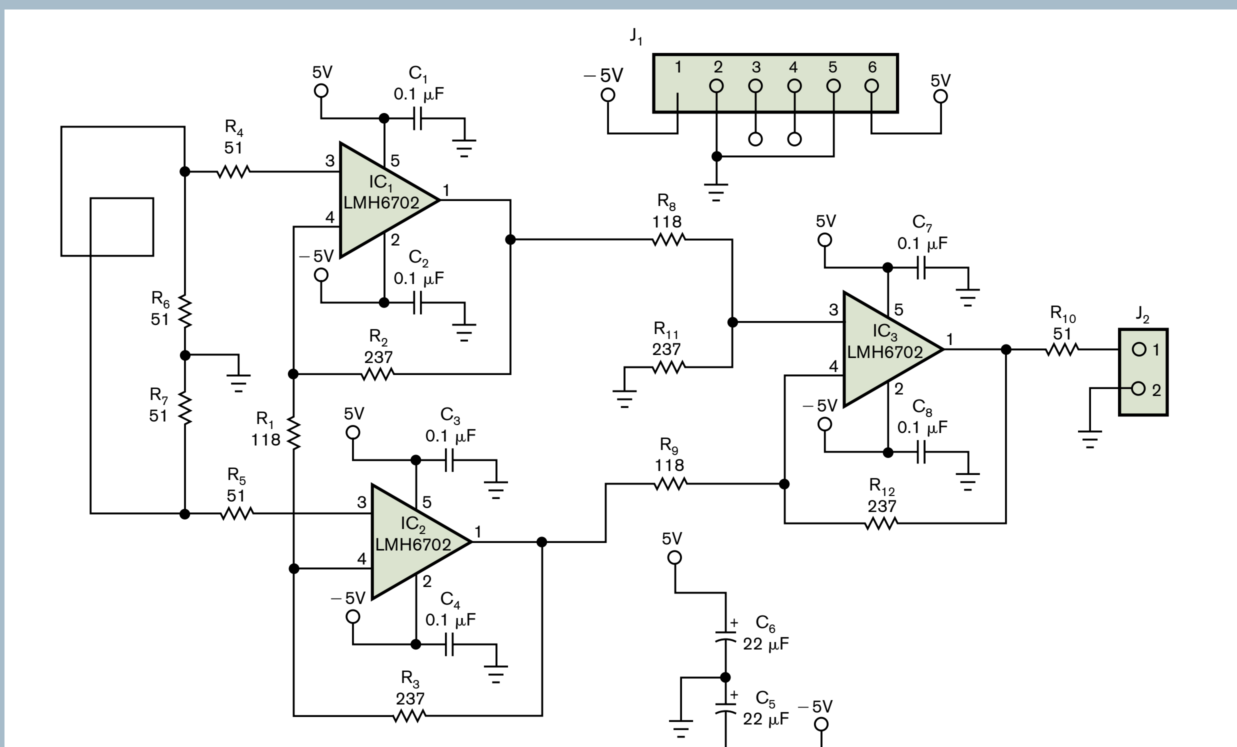


Figure A This high-bandwidth, 20-dB preamplifier amplifies the small signals that the magnetic loop picks up.

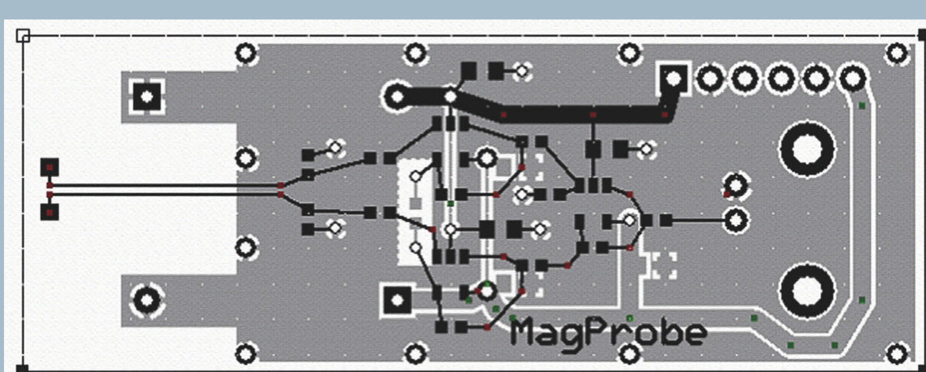


Figure B The amplifier layout is orthogonal to the probe tip and as balanced as possible.

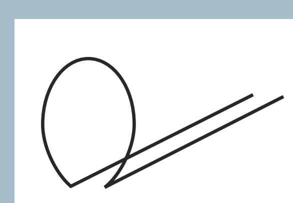
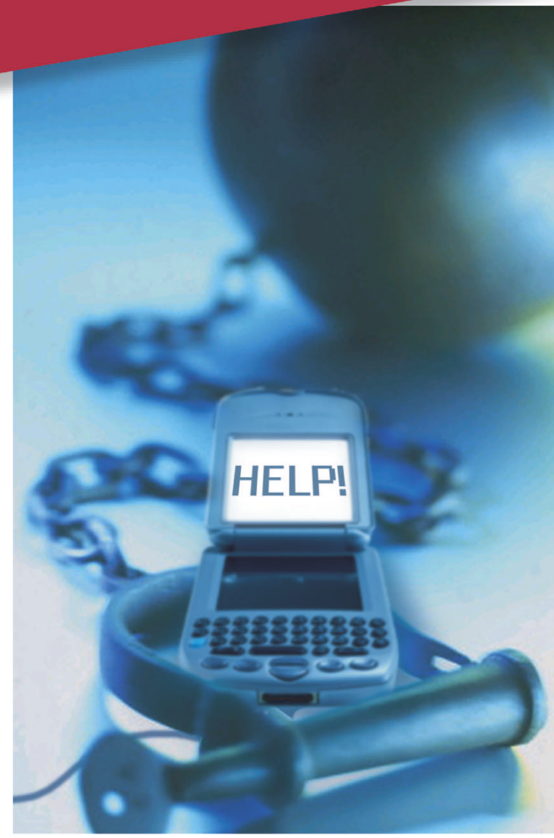


Figure C The probe tip provides a circular area 0.4 in. in diameter perpendicular to the circuitry on the pc board. A balanced input cancels any electric fields that couple to the probe tip.

Intersil Battery Charger ICs

Intersil High Performance Analog

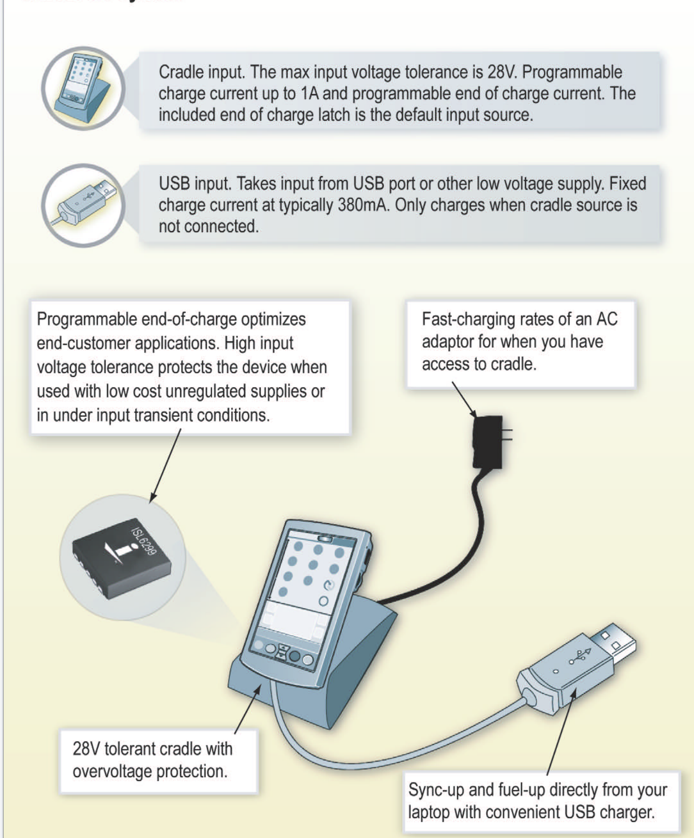


Unshackle Your Handheld Device

Intersil's ISL6299A is a fully integrated low-cost Li-ion or Li-polymer battery charger that accepts both USB port and desktop cradle charger.

The ISL6299A is a low component count solution that features programmable cradle charge current, charge indication, adapter present indication, and programmable end-of-charge (EOC) current with latch. All these advanced features, along with Intersil's Thermaguard™ technology for an added measure of thermal protection, are delivered in a single 3x3 mm DFN package.

ISL6299A System



ISL6299A Key Features:

- Dual-input charger for single-cell li-ion/polymer batteries for cradle and USB
- Low component count
- Integrated pass element
- Fixed 380mA USB charge current
- Programmable cradle charge current
- Charge current Thermaguard™ for thermal protection
- 28V maximum voltage for the cradle input
- Charge and adapter presence indicators
- Less than 0.5μA leakage current off the battery when no input power attached
- Programmable end-of-charge current with latch for cradle input
- No external blocking diode required
- Pb-Free plus anneal available (RoHS compliant)

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magnetic-flux density, and L is inductance. The **equation** says that you can induce an error voltage into a circuit by changing any one or more of the parameters. A given percentage change in current, magnetic field, or inductance (loop area) produces the same effect on induced voltage. Therefore, the design practice of reducing loop areas in high-performance circuits to eliminate errors from conducted emissions also reduces errors from magnetic coupling.

Although high-performance design practice dictates that you minimize loop area and shield necessarily susceptible components, such as filter inductors, it's always better to stop noise emissions at their source. Toward that end, instrument design-

CONVERTING VOLTAGE MEASUREMENTS TO MAGNETIC-FIELD DATA

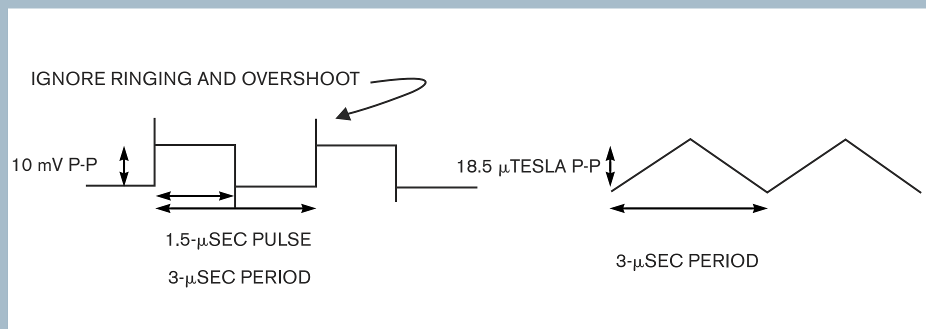

Figure A This typical time-domain measurement converted to the B-field is a 3-µsec, 50%-duty-cycle switching waveform. The 5-mV peak measurement equates to a 12.3-tesla/sec rate of change in flux density.

An instrument designer characterizing various sources of magnetic interference might find satisfaction with the relative-voltage measurements that a standard loop produces—assuming that the loop represents the loop area and orientation that an instrument might experience. But, because the loops and amplification can differ, it is helpful to convert these voltage measurements into field data.

Current in the emitting circuit creates magnetic flux that cuts through the test loop. The test loop is held stationary, including its angle to the field, θ, but the flux density, B, is changing to induce a voltage: $|V_{MEASURED}|=K_A A_L \cos\theta dB/dt$, where K_A is the gain of the amplifier, A_L is the area of the loop in square meters, dB/dt is the rate of change of the flux density in webers per square meter, or teslas. Plugging in the values and noting that the termination into the spectrum analyzer reduces the gain by a factor of two yields: $|dB/dt|\cos\theta=2467\times V_{MEASURED}$ (teslas).

Consider a reading of 10 mV p-p for the switching component in Figure A. Ignore the peak deviations at the switch transients because they do not add appreciably to the rms energy. This example has a 3-µsec, 50%-duty-cycle switching waveform. The 5-mV peak measurement equates to a 12.3-tesla/sec rate of change in flux density. Given that this rate remains 1.5 µsec, the flux density (B-field) in the direction of the pickup loop is 18.5 µtesla p-p.

You measure the magnetizing force, or H-field, in amps per meter, and you can determine it from the B-field by dividing by the permeability of free space, or $4\pi\times10^{-7}$. The 37-µtesla-p-p flux density is equivalent to 29.4A/m in an air-core circuit.

A spectrum analyzer can provide an alternative view of noise coupling. You can examine the issues of ringing and resonance. Reference A provides a derivation that takes advantage of a sinusoidal B-field: $V_N(\omega)=\omega K_A A_L B_R(\omega)\cos\theta$, where V_N and B_R are rms quantities at the frequency of interest, K_A is the amplifier gain, A_L is the loop area, and θ is the angle between the field vector and the area perpendicular to the loop area. Plugging in the previously determined values yields: $B_R \cos\theta=393 [V_N(f)/f]$ 2. For general application, you can convert this formula into a chart (Figure B).

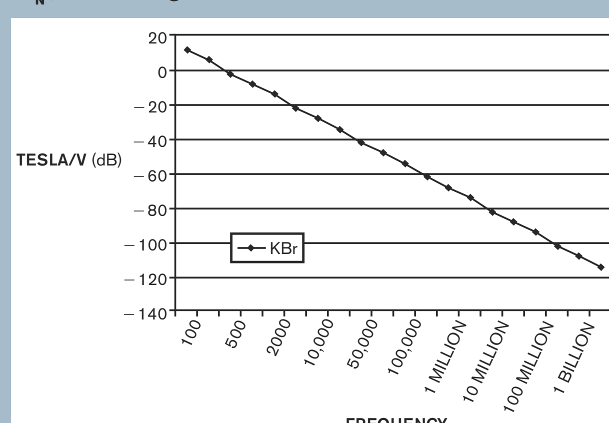

Figure B This chart shows the field-conversion factors for the magnetic probe.

REFERENCE

A Ott, Henry W, *Noise Reduction Techniques in Electronic Systems, Second Edition*, pg 38, John Wiley & Sons, 1988.

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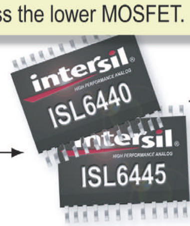

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ers would like to compare near-field performance in the time and the frequency domains before they select power converters for use in instruments. Magnetic-field specifications are not yet at this level of maturity, however, so device characterization is necessary.

MEASUREMENT EXAMPLE

For example, two similarly specified dc/dc converters have been characterized for magnetic-field emissions with a small loop antenna. Both converters are one-eighth-brick, wide-input-range devices using the same input voltage, 48V; output voltage, 5V; and load resistance, 4Ω. Both share the same conversion architecture—a fixed-ratio isolation stage following a regulation stage to support a 35 to 75V input range. These converters have two power magnetic sections within the design, but both run at the same frequency. Neither converter provides magnetic-emission data within the specification sheet.

In this characterization setup (**Figure 4**), a small pickup loop senses magnetic fields in the area above the dc/dc converters (see **sidebar** "Making your own magnetic-field-measurement

MAGNETIC CIRCUITS

Electrical engineers appear to be most comfortable working with circuits in which ideal conductors make signal connections. Inductors are OK for helping with frequency-domain issues, such as filtering, but there is a tendency to ignore the magnetic component.

Do not fear a magnetic circuit. Observing the similarities between inductors and capacitors is helpful in developing an understanding of the circuit operation (figures a and b and Reference A). The intensity of the electric field between the plates of a capacitor depends only on the voltage and the physical distance, d, between the plates: $E=V/d$ in volts per meter.

The intensity of the magnetic field surrounding a conductor depends only on the current and the physical width of the conductor, w: $H=I/w$ in amps per meter. The magnetic-field strength is sometimes called the magnetizing force.

Capacitance is a function of the plate area, the distance between the plates, and the dielectric material between the plates. The capacitance is $C=(\epsilon wl)/d$. The dielectric constant has units of farads per meter. A high dielectric constant produces more capacitance in a given plate area, holding plate separation constant, than a low dielectric constant.

A conductor forms a loop, creating an inductor. The inductance is a function of the area of the loop, the width of the conductor, and the permeability of the material surrounding the conductor: $L=(\mu dl)/w$. The core's permeability has units of henries per meter. Similar to the capacitor, high permeability produces more inductance in a given loop area, holding conductor width constant, than a material with low permeability.

In a capacitor, flux is a measure of the stored charge in coulombs. As the capacitor discharges, this charge becomes the source of current. Electric flux in a capacitor is a function of capacitance and voltage: $\Phi=CV$.

Magnetic flux in an inductor is analogous to the electric charge stored in a capacitor. Magnetic flux has units of webers and becomes the source of electromotive force (open-circuit voltage) as the inductor discharges. Magnetic flux is a function of the inductance and voltage: $\Phi M=LI$.

The dielectric that influences capacitance per unit also impacts flux density–or charge per unit area. Imagine flux lines between the positive and negative charges on the plate of the capacitor. The number of lines passing through a unit of area represents the flux density: $D=\Phi/(wl)=\epsilon E$. The flux density is directly proportional to the dielectric constant of the material between the capacitor plates.

The permeability of the core influences inductance and therefore magnetic-flux density. You measure flux density in flux per unit area: $B=\Phi M/(dl)=\mu H$.

REFERENCE

A Walker, Charles S, ***Capacitance, Inductance and Crosstalk Analysis***, Artech House, 1990.

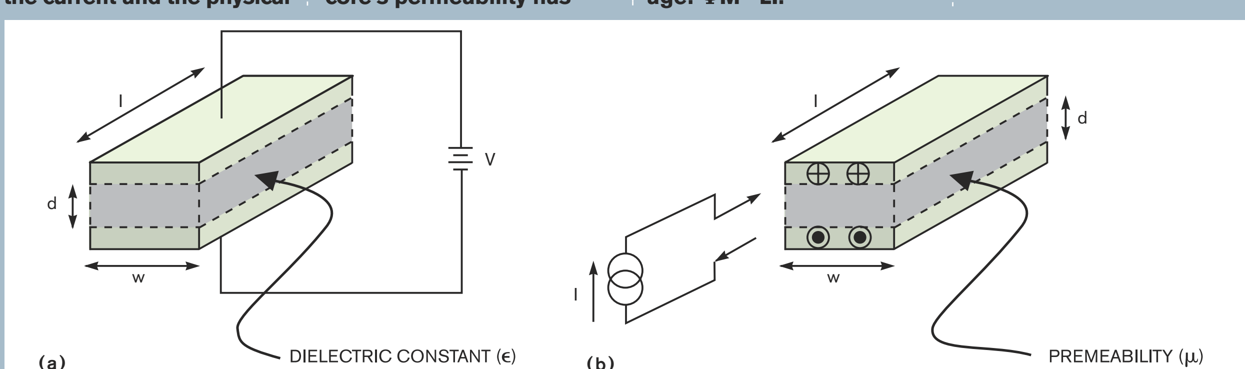

Figure A The electric field between the plates of a capacitor depends on the voltage and the distance between the plates (a). The inductance is a function of the area of the loop, the width of the conductor, and the permeability of the material surrounding the conductor (b).

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Total Output Power (W)		1200W/900W	1600W/1200W
Output Voltage	Vdc1	12	12
	Vdc2	3.3 or 5	3.3 or 5
Rated Output Current	Iout-1 (A)	98/73	131/98
	Iout-2 (A)	6/4	6/4
Input Voltage Range (VAC)		90-264	90-264
Isolation Voltage	Pri-Sec	3000Vrms	3000Vrms
	Pri-Chassis	1500Vrms	1500Vrms
PFC		Yes	Yes
Current Share		Active	Active
Efficiency		92%	92%
Features	HotPlug	Yes	Yes
	I²C	Yes	Yes
	EMI Class	Class A	Class A
	Airflow Direction	Back or Front	Back-Front
	Input Connector	IEC 320 C15	IEC 320 C20
	Output Connector	FCI PowerBlade #51732-021	FCI PowerBlade #51732-021
Dimensions (WxLxH)	Inches	4.75 x 12 x 1.6	4.75 x 12 x 1.6
	mm	120,6 x 305 x 40,7	120,6 x 305 x 40,7
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probe"). The amplified-loop output connects to an oscilloscope and a spectrum analyzer. The magnetic emission of the dc/dc converters contains a broad band of energy from the fundamental switching frequency that reaches to 50 MHz or more. It is important to treat the measured signal's distribution network as a high-frequency transmission line. The signal runs past the high-impedance oscilloscope input with a BNC tee at the scope input. The line terminates at the spectrum-analyzer input.

To best represent a victim circuit in a neighboring slot, orient the probe tip in a plane parallel to the converter's pc-board substrate. Scan the surface of the board for maximum output; the strongest field is above the isolation transformer (second stage). The intent of the measurements, which take place about 0.65 in. above the top surface of the transformer, is to place the pickup loop 1 in. above the plane that would represent the surface of the motherboard if you mounted the converter in an appropriate through-hole design (**Figure 5**).

Viewing measurement results in the time domain, you can see the converter's fundamental frequency and ringing frequency, and you can get a sense of the magnetic-field intensity (**Figure 6**). These converters demonstrate a trade-off in the converter's magnetic design. The isolation transformer's leakage and magnetizing inductance mutually couples to the measurement probe. Brand X has a significantly lower magnetizing inductance in its isolation transformer, as the higher fundamental field in the measurement shows. Brand Y has lower leakage inductance and therefore higher ringing frequency. The ringing that occurs around the switching transient is the result of leakage inductance and the switch's parasitic capacitance.

You can make two observations based on the derivative relationship of the earlier **equation**: A square-wave response means that the magnetic flux is changing linearly. The magnetic component is operating in a linear region, and current is increasing linearly. In broad terms, the magnetic field for Brand X is an 18-µtesla p-p triangular wave (see **sidebar** "Converting voltage measurements to magnetic-field data").

Although lower leakage inductance is better for reduced emission, the higher frequency resonance couples greater peak voltage at the higher frequency (**Figure 7**). A closer observation of the switching transient provides some insight into the resonance within the dc/dc converter.

If your main concern is for spectral interference in an ac-source or -capture instrument, you may be more interested in the information the spectrum analyzer provides. Taking a broad look at Brand Y's magnetic-field spectrum, you can see the resonance near 10 MHz and the components peaking at 20 to 25 MHz (**Figure 8**). **Table 1** summarizes the data from these samples.

Open-instrumentation architectures offer an important role for dc/dc converters. If the converters are not the sources of performance-limiting noise, they open a platform to a large set of applications. This article examines two similar converters using a high-bandwidth magnetic probe and finds different results. Because a system is only as quiet as its noisiest neighbor, anyone wishing to participate in open-instrument development should carefully evaluate to ensure a performance-compatible environment. EDN

AUTHOR'S BIOGRAPHY

William Bowhers teaches undergraduate electrical engineering at Merrimack College (North Andover, MA). His research follows a general interest in measurement technology that he acquired during 25 years of instrumentation development at Teradyne Inc (Boston). Bowhers received a master's degree in electrical engineering from Boston University (Boston) and a bachelor's degree in electrical engineering from Villanova University (Villanova, PA). He is a member of the IEEE and the American Society for Engineering Education.

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RAQ's

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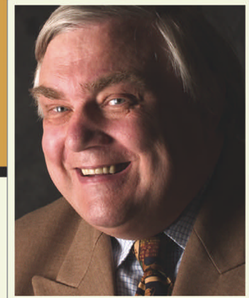
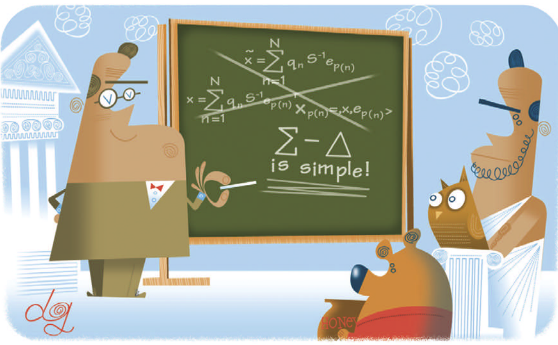


Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

It may be Greek to you, but sigma delta converters are not really hard to understand.

Q. *Can you please explain, simply, as to a Bear of Little Brain[1], how sigma-delta converters work?*



A. By over-sampling, noise shaping and digital filtering.

Athens is a beautiful city, with the ambiance of many millennia of history. I was walking round the Acropolis with Spiros, one of our Greek distributors, when he asked me how sigma-delta (Σ–Δ) converters work. "Sigma and delta are letters of our Greek alphabet," he exclaimed, "but every article I have seen about their operation is double dutch[2] to me. They all start with several pages of partial differential equations and then go downhill from there."

If a voltage is measured many times, the average of the measurements will be more accurate than most individual measurements. This is "over-sampling." (Dither[3] may be necessary to randomize the errors in the individual measurements.)

There is a definite theoretical minimum limit to the possible noise of an analog-to-digital converter (ADC). When an ADC samples a signal at a frequency of f_S the digital output contains the signal and this "quantization noise" is usually spread evenly from dc to $f_S/2$. By sampling at a higher rate of Kf_S, the noise is spread over the wider band from dc to $Kf_S/2$. If we then remove all the noise above $f_S/2$ with a digital filter the signal-to-noise ratio (SNR) of the digital output is improved — effectively improving the ADC resolution.

Normally the SNR increases with the square root of K, so very high sampling rates are necessary for useful increases in SNR. But a Σ–Δ modulator does not produce uniformly distributed quantization noise. Although the total noise is unaltered in a Σ–Δ system, most of it is at high frequencies (HF). This is known as noise shaping and permits much lower values of K.

If the digital output from the Σ–Δ modulator is filtered to remove HF, leaving the frequencies from dc to $f_S/2$ (where the wanted signals are) then the SNR and resolution of the digital output are improved. A Σ–Δ ADC simply consists of a Σ–Δ modulator and a digital low-pass filter, both of which are easily made with modern high-density digital technology. The principle of Σ–Δ ADCs has been known for more than 40 years, but the ability to build one on a chip is relatively recent.

---

1 *"When you are a Bear of Very Little Brain and you think of Things, you find sometimes that a Thing which seemed very Thingish inside you is quite different when it gets out into the open and has other people looking at it." — AA Milne, "The House at Pooh Corner"*

2 *Double dutch means gobbledygook*

3 *Dither — the addition of noise or some other AC signal in order to randomize errors.*

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PCI Express: Ever-faster graphics pipe serves many masters

THE NEW PCI EXPRESS SPEC SIGNIFICANTLY IMPROVES DESKTOP-PC GRAPHICS. DEVELOPERS ARE NOW WORKING ON GENERATION 2, WHICH WILL FURTHER EXPAND THE GRAPHICS PIPE.

The new PCI (Peripheral Component Interconnect) Express spec provides the biggest improvement in more than a decade in I/O performance for computation systems, significantly improving graphics in desktop PCs and workstations. Intel initially launched the spec in its chip sets in mid-2004, and the technology has become mainstream in high-end systems. But PCI Express is far more than an avenue to better games or video. As have many other PC innovations, PCI Express will enable significant applications, such as medical imaging, and serve in industrial control and many other embedded-system roles.

Serial PCI Express is usurping the parallel AGP (accelerated graphics port) in graphics as just one part of a broad industry trend toward serialization. For example, USB replaced the parallel and serial ports, and SATA and SAS (serial attached SCSI) are replacing parallel ATA and SCSI in storage interfaces. And, like parallel PCI, PCI Express will handle far more than graphics, providing a flexible and scalable data highway for all types of performance-centric add-on functions.

You might ask whether a replacement for PCI-derived AGP is necessary. AGP8× pushed the evolutionary limits of what was possible with a parallel bus—at least at a price point sustainable for volume PC production. Clock skew was the problem plaguing AGP, like other parallel buses touting higher performance. A single clock defines the data-valid period across AGP's 32 data lanes. But the faster the clock runs, the narrower the data-valid window becomes, and the tougher the design challenge becomes (see **sidebar** "History of the graphics pipe").

So, the graphics pipeline became serialized with PCI Express. This serialization means that data carries with it an embedded clock, which a PLL recovers in the receiver circuits. Multiple lanes can carry data in parallel, providing scalable performance, but each lane has its own embedded clock (**Figure 1**). At the receiver end, the data resynchronizes. PCI Express can tolerate as much as four symbols of skew between lanes, dramatically easing the constraints for motherboard and graphics-controller design.

PCI Express is more than just the follow-on to AGP. PCI Express is also the migration point for applications currently on conventional PCI and PCI-X as they move to higher speeds and performance. These legacy buses will not go away overnight, but, like ISA (Industry Standard Bus), they eventually will. PCI Express reunites the forks that broke away from the original PCI with a common protocol and electrical interface. Moreover, PCI Express technology will make its way to the embedded-system world in CompactPCI implementations.

For graphics implementations, the PCI Express bus comprises 16 lane pairs. Each lane pair has four data wires—a transmitting differential pair and a receiving differential pair. Because PCI Express is dual-simplex, data can flow in both directions unimpeded by data going the other direction, unlike AGP (**Figure 2**). AGP was point-to-point like PCI Express, but AGP

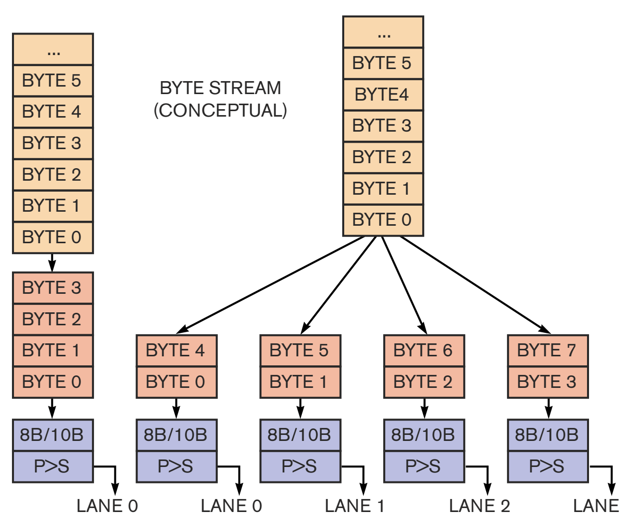

Figure 1 The PCI Express offers scalability through the concept of lanes. Designers can linearly extend bandwidth by adding lanes. In a one-lane system, such as Lane 0, the data bytes flow sequentially as expected. In a multilane scenario, the bytes are interleaved across the lanes for transmission.

is full-duplex: Data can flow in only one direction at a time. Furthermore, AGP never offered symmetric bandwidth in its implementations, even though nothing about the AGP protocols precludes symmetry. AGP8× achieves 2.1-Gbyte/sec peaks in data flows from the host CPU to graphics controllers, which is the primary direction for graphics traffic. However, in typical system implementations, the real available "back-channel" bandwidth is about one-tenth of that figure. In contrast, PCI Express graphics offers 4-Gbyte/sec peak bandwidth simultaneously in both directions and, in typical implementations, delivers the bulk of that bandwidth in both directions. This highly symmetric bandwidth leads to some interesting new capabilities for graphics based on PCI Express and in many other I/O applications.

AGP implementations yielded weak back-channel bandwidth for several reasons. To achieve the best CPU-to-graphics controller performance, AGP worked from uncached address spaces (the AGP "aperture"). For reads, this assumption makes perfect sense, because caching requires snooping, degrading performance. However, chip-set designers simply did not optimize their chip sets for large data-set writes to this space from the graphics controller because the cost of providing a large number of write-posting buffers was prohibitive. This trade-off made sense

IN THE DEFINITION OF PCI EXPRESS, THE GRAPHICS INDUSTRY WAS UNANIMOUS IN THE OPINION THAT IT DIDN'T WANT SIMILAR "HELP" IN THE NEW I/O INTERFACE.

to the chip-set architects, because graphics traffic is primarily in the forward direction.

A second reason for the relative weakness of AGP's back-channel bandwidth was a limitation in the GART (graphics-address-remapping-table) memory-management system that AGP provided to assist in the graphics controller's task of managing physical- and virtual-address translations for access to uncachable system-memory space. Again, the theory sounded great, but practical design considerations led to suboptimal graphics performance, because real chip sets never implemented enough TLBs (translation-look-aside buffers). Each 4 kbytes of memory requires a new TLB because 4 kbytes is the default page size in Windows. But even two dozen TLBs support only about 100 kbytes of memory before the onset of TLB "thrash."

HISTORY OF THE GRAPHICS PIPE

The demands of graphics were the primary driving force behind the PCI (Peripheral Component Interconnect) bus. The developers of the original ISA (Industry Standard Bus) based it on the PC AT's Intel 286 processor bus, which debuted in 1984. ISA delivered only 16 Mbytes/sec at 8 MHz, and was woefully inadequate for the fire hose of data that 3-D graphics requires. The VESA (Video Electronics Standards Association) developed the VL (Video Local) Bus as a proposed alternative to ISA. EISA (Extended ISA) was another. The VL Bus designers were clever in getting more than 100-Mbyte/sec bandwidth from the CPU to the graphics controller. However, the bus worked only on graphics because it did not support multiple devices. Furthermore, it tied only to a specific processor's bus and, thus, could not adapt to future technologies. These facts explain why PCI, with its 133-Mbyte/sec bandwidth, triumphed over a 32-bit, shared, "multidrop" bus. Intel in 1991 proposed PCI as a scalable replacement for ISA and helped form the PCI-SIG (special-interest group), which in 1993 released the first specification.

You'd think the graphics industry would happily chew on this order-of-magnitude increase in bandwidth for a while, but that scenario didn't occur. During that era, Microsoft (www.microsoft.com) moved from DOS to Windows, causing a discontinuity in demand for 3-D-graphics capabilities in PCs. Intel in 1997—only three years after PCI entered production—introduced its Pentium II processor with the AGP (accelerated-graphics port). AGP borrows heavily from PCI technology. AGP is also 32 bits wide, and its protocols build on top of PCI protocols. But AGP is a nonshared, point-to-point bus. It uses a different connector from the one that PCI uses. And, although PCs would commonly have four to six PCI slots, they would have only one AGP slot.

AGP went through many speed bumps to achieve 2.1 Gbytes/sec in its AGP8× version, which its developers released in 2002, a remarkable evolution from its roots in PCI. You'd think the graphics community would be happy now, having fattened the pipe nearly three orders of magnitude in only two decades. However, graphics vendors believed they'd be taxing this bandwidth within a few short years.

PCI Express began life as 3GIO (third-generation I/O) in the Arapahoe Work Group but moved quickly to become a specification that the PCI-SIG owned. That group in July 2002 released the 1.0 Version. First desktop, workstation, and server products from Intel went into production mid-2004, and the first chip sets for notebooks debuted early in 2005. Now, a range of PCI Express products are available in many categories of devices (Reference A).

REFERENCE

A Intel Developer Network for PCI Express Architecture, www.pciexpressdevnet.org/kshowcase.

A cache thrashes when its miss rate is too high, and it spends most of its time servicing misses. Thrashing, particularly virtual-memory thrashing, is bad for performance, because the relative cost of a miss is so high: It may slow a machine down by a factor 100 or more.

In the definition of PCI Express, the graphics industry was unanimous in the opinion that it didn't want similar "help" in the new I/O interface. With PCI Express graphics, all memory management occurs within the graphics controller. Memory-management performance is under the control of the graphics vendors, who are more economically motivated in general than are chip-set vendors to spend gates on graphics performance.

At this point, it is reasonable to ask why continually increasing the bandwidth of the pipe from the host CPU to the graphics controller is so important. More prosaically, an end user may reasonably want to know what he can do with a notebook, desktop PC, or workstation with PCI Express graphics that is not possible with AGP8× or, for that matter, what PCI Express offers in embedded-system roles. Only a few of today's applications are starting to top the limits of what AGP8× can deliver. It is not difficult to create a demo application that uses the full bandwidth of PCI Express, and the suppliers of graphics controllers use this approach to show off their latest products. But broadly available commercial applications rarely show any advantage just from the fatter pipe when the pipe enters.

The PC world still needs PCI Express graphics, and end users have good reasons for desiring them. To understand this concept, consider the perspective of a developer of graphics-intensive software, such as that for video games or CAD. These developers write their programs to the capabilities of the least-common-denominator hardware in their target customer base. For leading-edge video games and high-end-workstation applications, these hardware units are highly capable, recently introduced systems, but more generally the target is likely to be systems the vendors released over the last two to four years.

The only way to get the software community to continuously raise the bar in graphics capabilities is by continuously increasing the capabilities, including bandwidth, of the client platforms. The impact of AGP8× on software development is happening now. The work to bring PCI Express to market will have its major impact on software applications in the future.

But the end user still has plenty of incentive to purchase PCI Express graphics today. A buyer of PCI Express graphics is well-prepared for the getting the most from the new applications that emerge over the life of that PC. And, second, the suppliers of

THE ONLY WAY TO GET THE SOFTWARE COMMUNITY TO CONTINUOUSLY RAISE THE BAR IN GRAPHICS CAPABILITIES IS BY CONTINUOUSLY INCREASING THE CAPABILITIES, INCLUDING BANDWIDTH, OF THE CLIENT PLATFORMS.

graphics controllers are focusing their latest developments on PCI Express products. So, the client with PCI Express graphics will likely significantly outperform previous generations of products, even if PCI Express cannot, in general, now take credit for that performance advantage.

The performance advantages of PCI Express graphics may emerge more quickly than with previous transitions because of the tremendous increase of CPU performance and memory bandwidth just coming to market. For example, the latest Intel workstation platform exploits as much as 64 Gbytes of fully buffered DIMM with a peak bandwidth of 21 Gbytes/sec. Conjoin those features with additional capabilities in the most recent graphics controllers, and you can more fully exploit the bus.

PCI Express affords system designers an extremely broad range of capabilities. In the graphics world, PCI Express dual-graphics controllers are popular with gamers. Some designers are even contemplating externally cabled PCI Express subsystems (see **sidebar** "Express outside the box" and the online **sidebar** "Dual controllers accelerate rendering" at www.edn.com/ms4201).

REAL-WORLD ADVANTAGES

PCI Express is a key enabler in some lifesaving applications. For example, consider Vital Images (www.vitalimages.com), a leading provider of enterprisewide advanced visualization and analysis software for use in disease-screening applications, clinical diagnosis, and therapy planning. The company's technology gives radiologists, cardiologists, oncologists, and other medical specialists timesaving productivity and communications tools for easy use in the day-to-day practice of medicine. Vital Images' software products include a medical-diagnostic tool that allows physicians to use PCs or notebook computers to gain remote access to 2-, 3-, and 4-D advanced visualization. The software enables users to measure, rotate, analyze, and segment images.

One technical challenge for this medical application stems from the size of data sets that volumetric visualization requires. According to Karel Zuiderveld, PhD, director of technology research at Vital Images, "PCI Express is especially beneficial when dealing with large data sets that do not fit into graphics memory. The size of modern medical data sets, [which the company obtained using computer-tomography], range from hundreds of megabytes to several gigabytes. In addition to a vast amount of CPU and GPU [graphics-processing-unit] resources, fast rendering of such data sets also

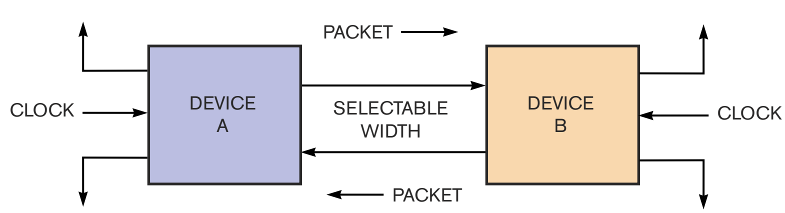

Figure 2 PCI Express implements a full-duplex link in which traffic flows symmetrically and simultaneously in each direction over serial links with the clock embedded in the data.

requires high transfer speeds to the GPU." With PCI Express graphics, medical professionals can view 3-D images from alternative perspectives with reasonable response times.

In the past, the graphics bus has not been the bottleneck. When uploading textures to OpenGL, the driver usually "swizzles" the texture—that is, swaps the pixels around so that they are stored in the same way as the original format. It then creates a copy in system memory, according to the OpenGL spec, and writes a copy to the graphics memory. Until recently, the CPU usually performed texture swizzling, resulting in low texture-upload speeds. Each texture requires a read-swizzle-write memory DMA to the graphics card; this approach involves at least two reads and one write to system memory. With the latest workstations, Vital Images' target applications may fully exploit the bandwidth of PCI Express, says Zuiderveld. Though medical imaging may be a leading application for taxing the PCI Express bus, he believes that the trend toward using resources such as the virtual texture maps that Microsoft's (www.microsoft.com) DX10 supports, will drive steeply increasing usage of PCI Express's graphics bandwidth into mainstream applications.

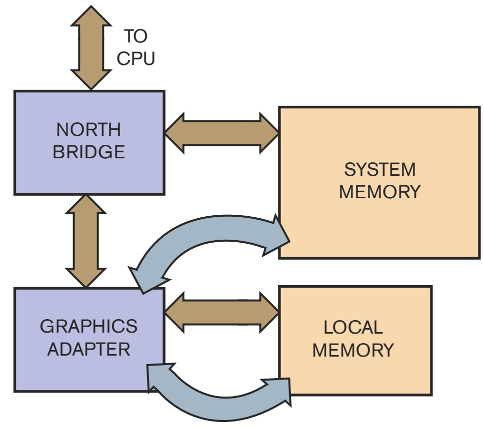

Figure 3 Nvidia and ATI with their TurboCache and HyperMemory technologies, respectively, use the PCI Express bus back channel to effectively cache their local memory (courtesy ATI).

EXPRESS VIDEO EDITING

One application that can now take advantage of PCI Express' unique capabilities is video editing. In video applications, PCI Express affords dramatically better back-channel bandwidth than AGP. Back-channel rates are important, because main memory must store intermediate and temporary video-processing results. The files are just too large for the graphics controller's local store. However, the memory must preserve this data without lossy compression, because the cumulative effects of repeated compressions would visibly degrade the end result. With AGP, these writes of uncompressed data back to main system memory are major performance bottlenecks that PCI Express relieves. Watch for video editors that take advantage of PCI Express to enter the market.

PCI Express is backward-compatible with PCI protocols but offers numerous features that go beyond the PCI protocols. One feature—isochrony, or equality in length of time—promises to further aid video editing and other heavily multithreaded applications. PCI and AGP provide no guarantee for worst-case latency. Particularly in commercial-scale video editing for broadcast and film, this lack of guarantee for data delivery creates difficult challenges when trying to maintain output at a given frame rate. Isochrony could also ensure that systems running many multithreaded concurrent applications don't drop display frames. As chip-set and device-hardware vendors and operating-system upgrades add isochrony support, PCI Express will provide this guarantee that AGP could not.

Some graphics vendors have already figured out how to exploit PCI Express' back-channel bandwidth to create a new class of products. Before PCI Express, graphics memory was either in system memory—for chip sets with integrated graphics—or on an external card with an external graphics controller. Though AGP's developers intended it to support heavy use of system

EXPRESS OUTSIDE THE BOX

An ongoing development in the PCI-SIG (Peripheral Component Interconnect Special Interest Group) that potentially relates to PCI Express graphics is the definition of a PCI Express cable. PCI Express intends to provide an I/O-attachment point for a host, not to be that I/O itself. The developers of PCI Express had no intention of competing with cabled-I/O interfaces, such as USB, FireWire, Ethernet, InfiniBand, and others. However, a cable allows the extension of the I/O-attachment point to be remote from a host system. A cable adapter card could plug into a 16-card slot and cable externally to a remote 16-card slot. Depending on distances and adherence to all the PCI Express design rules, this card might get away with containing no active circuitry, or it might contain a PCI Express switch or bridge that acts as a signal repeater.

One intriguing possibility would be a cable adapter card connecting, through a PCI Express cable, to a remote box containing a switch that supports two 16-card slots. Using a 48-lane switch, you could fully provision both of these slots and deliver a spec-compliant option. Such a remote dual-graphics box might afford some additional advantages. For example, by removing the graphics controllers from the base system, it also removes their power and thermal requirements from burdening the base system. Also, any client with just one 16-card slot becomes "dual-graphics capable." Such a remote dual-graphics box might prove attractive to OEMs that do not perceive dual graphics to be a mainstream requirement but want to provide their customers the capability and an upgrade path. It also might make an attractive after-market product.

memory, especially for textures, actual AGP implementations failed to deliver sufficient performance. The performance gap was too great between implementations with local frame memory on the graphics card and implementations using the AGP bus to access system memory. So, either you integrated graphics in a chip set, or you put a lot of graphics RAM on the external controller. A significant price and performance difference exists between these two approaches. Nvidia (www.nvidia.com) and ATI (www.ati.com) with their TurboCache and HyperMemory technologies, respectively, use the PCI Express bus back channel to effectively cache their local memory (**Figure 3**).

This method provides lower performance than that of a large local memory store on the graphics card, although the performance decrease does not approach the degradation that would occur on AGP. Still, these caching technologies allow the removal of significant amounts of RAM from the graphics-controller card. Instead of, say, eight 8-Mbit×16-word DDR DRAMs for a traditional, state-of-the-art graphics controller, the controller card using caching over PCI Express could use just a single 4-Mbit×32-word DDR DRAM. Memory costs would drop from approximately $16 in today's prices to $3.50, and performance would still be better than that of integrated graphics.

The future of PCI Express graphics does not end here. The PCI-SIG (special-interest group) has announced work on a Generation 2 version of PCI Express. Though the specification was under development at press time, the PCI-SIG has announced key aspects of the new version. It will double the clock rate to 5 GHz. The group doesn't plan significant protocol enhancements over PCI Express 1.1, and Generation 2 will be backward-compatible with PCI Express 1.1. The PCI-SIG suggests that Generation 2 could be in production in 2007. When it does arrive, Generation 2 PCI Express will continue the grand tradition of regularly expanding the graphics pipe between host and graphics controller that you have witnessed from ISA to PCI to AGP and now to PCI Express. EDN

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AUTHOR'S BIOGRAPHY

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LINEAR TECHNOLOGY DESIGN NOTES

Handheld High Power Battery Charger

Design Note 393

Mark Gurries

Introduction

As the performance of many handheld devices approaches that of laptop computers, design complexity also increases. Chief among them is thermal management—how do you meet increasing performance demands while keeping a compact and small product cool in the user's hand?

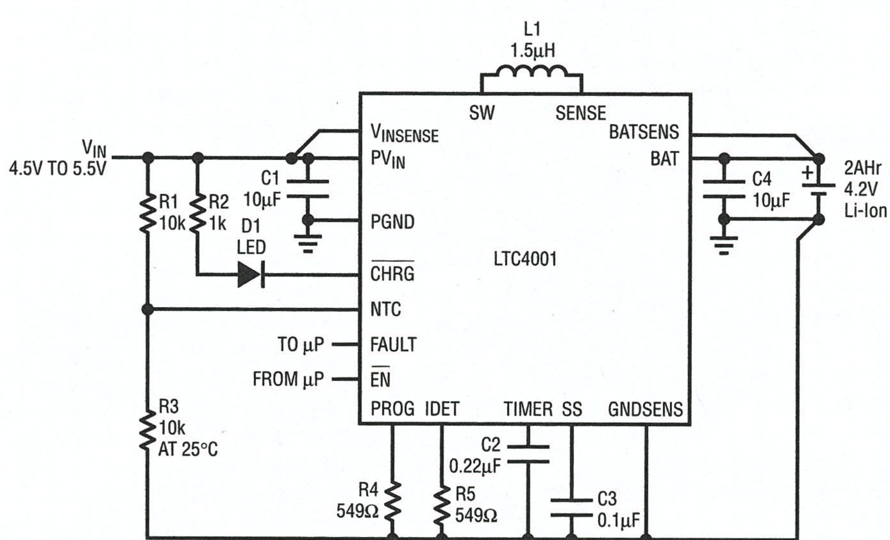
For instance, as battery capacities inevitably increase, charge currents will also increase to maintain or improve their charge times. Traditional linear regulator-based battery chargers will not be able to meet the charge current and efficiency demands necessary to allow a product to run cool. What is needed is a switching-based charger that takes just about the same amount of space as a linear solution—but without the heat.

Small PCB Footprint

Figure 1 shows how simple a feature-laden LTC®4001-based charger solution can be. This switching-based charger only requires the IC, a small 1.5μH inductor, two small 1206-size 10μF ceramic capacitors, and a few other tiny components. Furthermore, even simpler configurations are possible (see Figure 2). This monolithic 2A, 1.5MHz synchronous PWM standalone battery charger is packaged in a 4mm × 4mm 16-pin QFN package, which contains the built-in switching MOSFETs and charge termination controller. Figure 3 shows an actual PCB solution.

Advanced Features and Functions

One of the more unique features of the LTC4001 is its full remote voltage sense capability which permits faster charge rates by bypassing voltage drops in narrow PCB traces, EMI filters or current sense resistors for gas gauge related support; this is placed on the system side of the battery connector. Eliminating these losses in the sense circuit can significantly shorten the constant voltage phase of the overall charge time.



L1: VISHAY DALE IHLP-2525AH-01
R3: NTC VISHAY DALE NTHS0603N02N1002J

Figure 1. Li-Ion Battery Charger with 3-Hour Timer, Temperature Qualification, Soft-Start, Remote Sensing and C/10 Indication

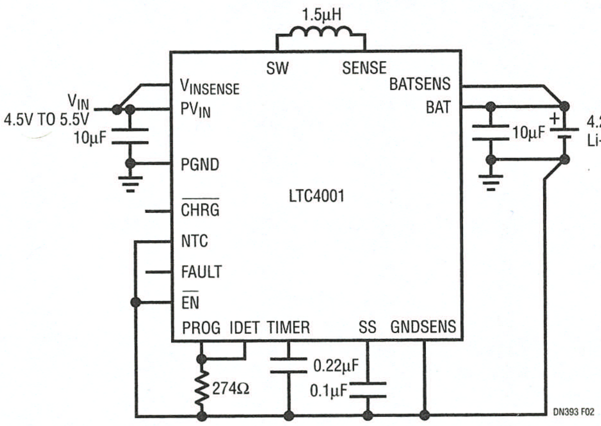


Figure 2. Simple 2A Battery Charger

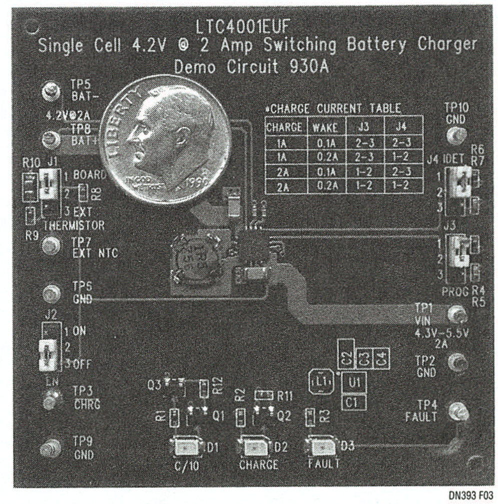


Figure 3. Actual LTC4001 Demo Board Showing a Compact Footprint (Height ≤ 1.8mm)

Another important feature is programmable soft-start, which requires only a small ceramic capacitor on the SS pin. Soft-start saves design time and cost by simplifying the power source requirements, precluding the need to handle fast start-up load transients commonly found with switching power supplies.

Other advanced features include: 50mA trickle charge recovery of over-discharged batteries below 3V/cell; adjustable charge timer via a single capacitor on the TIMER pin; and automatic restart of a charge cycle when the battery voltage falls below 100mV of the full charge voltage.

Two signals provide status. First is the FAULT pin, which in conjunction with the LTC4001 thermistor circuit, reports an out-of-range temperature situation. When a temperature fault occurs, the charge process is stopped immediately. Charging a battery when it is out of its normal temp range can damage it. Second, the $\overline{\text{CHRG}}$ pin shows three states relating to the charge state of the battery or charger. In addition to the normal OFF indication, it also indicates when the battery is below its user programmable I_{DET} threshold or when in bulk charge mode.

The $\overline{\text{EN}}$ (Enable) pin allows for shutdown of the charger, thus reducing its V_{IN} quiescent current below 50μA and the battery drain current to less than 3μA. Shutdown also occurs automatically if V_{IN} falls to less than 250mV above the current battery voltage.

Flexible Options

The LTC4001 provides a number of flexible options in its small package. Bulk charge current is programmable via the PROG pin and a simple resistor, from 2A and below. A separate resistor on the I_{DET} pin is all that is required to set the full charge current termination or indication threshold independently of the bulk charge current setting. Typically the I_{DET} threshold is set to 1/10 (C/10) of the bulk charge current, which equates to a battery being about 95% to 98% full. Raising the I_{DET} current trip threshold significantly reduces charge time by having a full charge indication occur sooner in exchange for a slightly lower full state of charge. Likewise, increasing the trip threshold extends the timer to approach a 100% state of charge if there are no serious time constraints. The type of charge termination is also flexible. In addition to timer-based termination, the charge can be terminated when the I_{DET} threshold is reached or charge termination can be defeated all together to allow an external power manager to decide.

Conclusion

The LTC4001 is the charger of choice for the next generation of handheld devices with its tiny solution size, unmatched power capability, high efficiency, protection features and flexible options.

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LINEAR TECHNOLOGY

Microprocessor generates programmable clock sequences

William Grill, Honeywell BRGA, Lenexa, KS

To produce trains of pulses suitable for keying transmitters, testing circuits, and debugging data links, designers requiring continuous or event-driven pulse sequences have traditionally relied on pulse generators or collections of simple circuits. Today's inexpensive microprocessors make it possible to design and build low-cost, dedicated pulse-sequence generators with a minimum of resources. In a small, SOT-23-packaged, 10F200 controller from Microchip (www.microchip.com), the design in **Figure 1** uses a code-based embedded table algorithm to generate an application-settable period and table-based PWM (pulse-width-modulation) sequence. The application produces a continuously pulsed sequence and requires only three constants and a pulse-width profile table that it copies into the microprocessor's assembler-based code before compiling (**Figure 2**).

All code branches undergo equalization to produce a group of 29 constant instruction times. During software development, you can use coded constants and a table-based approach as a flexible method of modifying the pulse sequence. The three parameters that **Figure 2** highlights include the number of PWM cycles that execute between tabled steps, which the algorithm passes as "temp_cntK." This parameter defines how many PWM periods of a range from one to 255 repeat within each tabled step. For three cycles per table step, you use #define temp_cntK .3. The next parameter is the number of 29-instruction loops that execute during each PWM period. All branches of the coded instructions equalize to constant 29-instruction periods. When you copy this parameter as "loopsK," it can range from one to 255. Using the 10F200's internal 4-MHz clock and an 8-bit counter to generate 1-μsec instruction periods, you can generate a PWM period range of 58 to 7395 μsec, which corresponds to a frequency range of 17,241 to 135 Hz. For a 1-msec PWM-cycle period and the sequence in **Figure 2**, you require 31 base loops per cycle, which you obtain by dividing 1 msec by the 29-μsec instruction period: #define loopsK .31.

You then equate the total number of table profile steps to "table_maxK." The total number of profile steps that a look-up table includes and that you copy into the code may vary from one to 252. In this application, five tabled steps correspond to pulse duty cycles of 25, 50, 87.5, 12.5, and 75%. These val-

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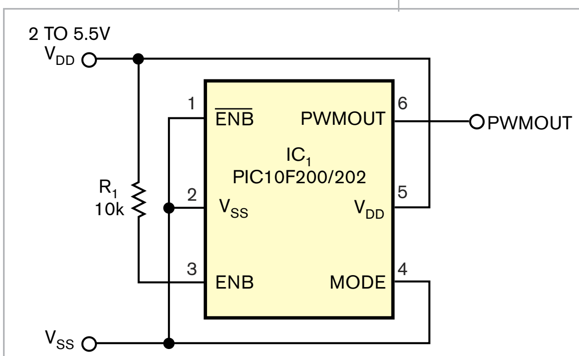

Figure 1 A microcontroller and a resistor can deliver a complex PWM output.

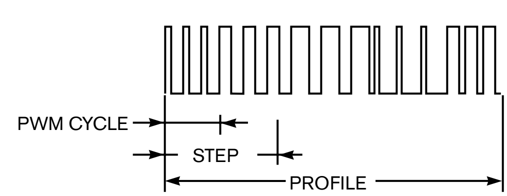

Figure 2 This waveform profile comprises five steps, each using one of three PWM cycles. In continuous mode, the circuit's output repeats indefinitely.

ues undergo scaling according to the following **equation**: Duty cycle=INT (%T_{DTY}/100×loopsK+0.5), in which INT is the integer value and %T_{DTY} is the percentage of the total duty cycle. In this example, loopsK=31. The number of steps in the table passes to the program as #define loop_maxK .5.

The pulse-duty cycle can vary only in increments of a single 29-instruction base loop, and, as a consequence, the pulse duty cycle's resolution varies as the number of basic loops for the waveform's desired period, which you define as loopsK=31 loops. Thus, the duty-cycle resolution equals 1/(loopsK), or 1/(31)=3.22% for this application.

You can use a spreadsheet or manually calculate the translated and scaled duty-cycle values and store them in the data-profile table. For example, you calculate the value for a 25% duty cycle as INT(25/resolution+0.5)=INT(25/3.22+0.5), where INT represents extraction of the integer value of the computed quantity. For required duty cycles of 25, 50, 87.5, 12.5, and 75%, the values that pass to the data-profile table are retlw_8, 16, 27, 4, and 23, respectively. The assembly-language program available for downloading from the online version of this Design Idea at www.edn.com/060720di1 includes these duty-cycle values and the three other parameters.

The program includes two additional features: Connecting Pin 1 to ground enables a continuous-output mode. Connecting Pin 1 to $+V_{DD}$ evokes a single output waveform. Pin 3 serves as a high true-output enable when you connect it to $+V_{DD}$ or as a positive-edge trigger input when you pull the pin to ground and release it. Note that the program currently includes no contact-debounce routines for either input.

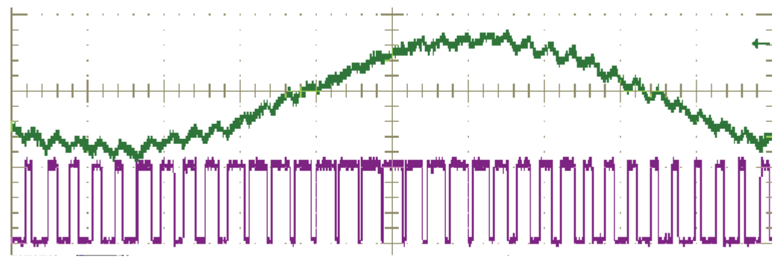

Figure 3 After undergoing lowpass-filtering, the controller's pulse-width-modulated output (lower trace) reveals its sine-wave origin.

In the example in **Figure 3**, the controller delivers a pulse-width-modulated output (lower trace), which, after processing by a single-pole lowpass filter, corresponds to a sine wave (upper trace). Using another version of the circuit, you can evaluate how a critical midword error affects a serial link's characteristics, system timing, and response latency.

The waveform in **Figure 4** comprises 100 pulses, 99 of which exhibit a nominal duty cycle that varies from 48 to 51%, and a single error pulse with a 75% duty cycle. The waveform-table entries use values of loopsK=100, temp_cntK=1, and table_maxK=100 to produce a pulse sequence comprising 74 pulses with nominal duty cycles, a single pulse with a 75% duty cycle, and a final sequence of 25 clocks with nominal duty cycles. The entire sequence repeats at a 345-Hz rate.

Using a 4-MHz-clock-rate version of Microchip's 10F220 controller constrains the basic software-timing loop to a 29-μsec period. You can compile the program into an 8-MHz 10F220 to reduce the timing loop to 14.5 μsec and extend the output's usable bandwidth. You can modify the code in the **listing** to suit other compatible microprocessors to obtain greater bandwidth and integrate additional functions. As is, the circuit requires only 155 bytes of internal EEPROM and occupies an SOT-23 pc-board footprint—not bad for a processor that costs less than $1. EDN

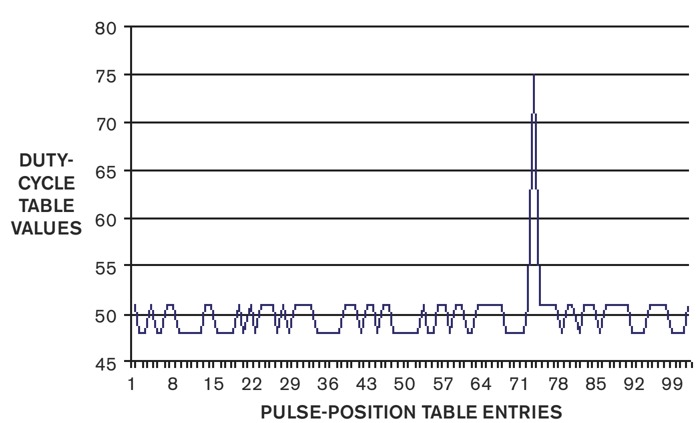

Figure 4 Devised for testing a serial link's error response, this waveform plot displays pulses' locations within the waveform (horizontal axis) versus the duty cycle for each pulse (vertical axis). The waveform cycle repeats after pulse 100 ends.

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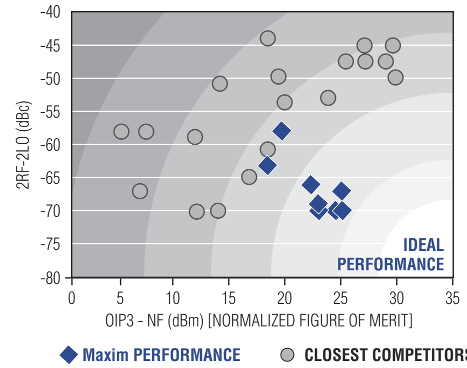

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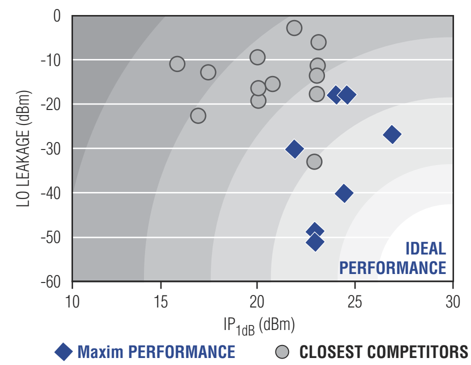

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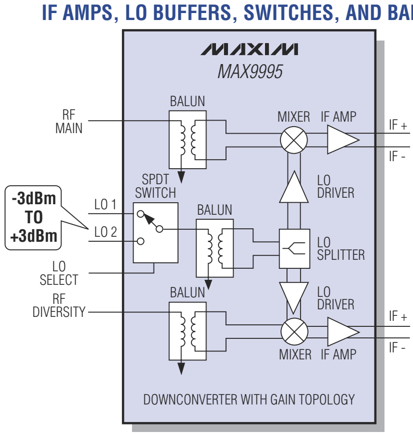

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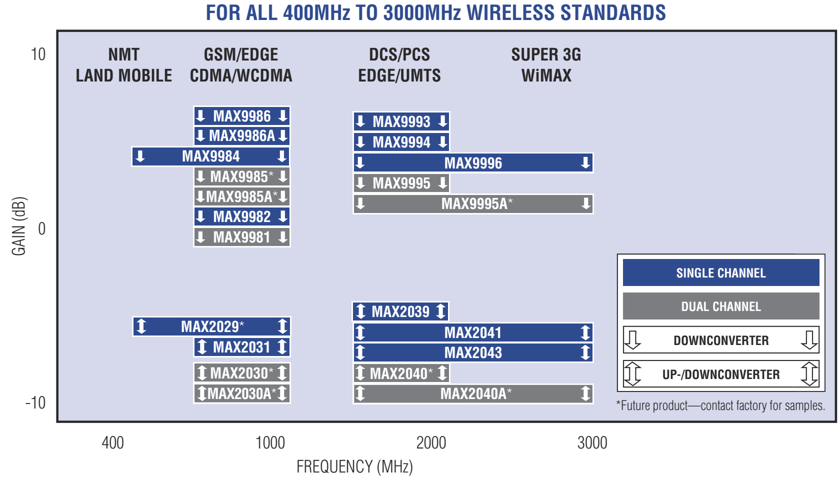

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Ceramic output capacitors enhance internally compensated switchers

Robert Kollman, Texas Instruments, Dallas, TX

Integrating compensation components with a power-supply controller and buck regulator's power switches can minimize pc-board area, improve reliability, and eliminate assembly errors by reducing the number of components and solder joints. However, integration also limits a designer's range of choices in the selection of output-filter components. **Figure 1a** presents a typical switching regulator based on Texas Instruments' (www.ti.com) TPS5430. The boxed area in **Figure 1b** shows a simplified version of the IC's internal small-signal-equivalent circuit, which includes an error amplifier, E_1; passive-compensation components; and a voltage-controlled voltage-source, E_2, which represents the modulator and the power switches. Support components external to the IC include output-filter components and their parasitic resistances, a resistor representing an external load, and a divider comprising R_1 and R_2 that sets the output voltage. The compensation-circuit design accommodates a certain range of output-filter inductance and capacitance and their associated parasitics.

Figure 2 shows Bode diagrams for the error-amplifier and modulator-gain blocks (**2a**) and the entire regulator system (**2b**). Envisioning that end users would specify aluminum electrolytic capacitors for the output-filter circuit, the IC's designer includes a Type 3 compensation circuit to optimize the IC's performance for aluminum capacitors' characteristics. Note that a Type 3 compensation circuit includes a pole at the origin of the circuit's pole-zero plot to provide high gain at dc and an integratorlike high-frequency roll-off augmented with pairs of poles and zeros to provide phase and gain margins at certain frequencies (**Reference 1**).

The regulator's LC-output modulator/filter's amplitude-response curve peaks at the resonant frequency set by the filter's inductor and output capacitor, and then it decreases at a −40-dB/decade rate until it reaches a zero at a frequency set by the output capacitor and its ESR (equivalent series resistance). Beyond that frequency, the output inductor's and the capacitor's ESRs determine the attenuation curve's slope, resulting in a −20-dB/decade rate.

For good regulation, the error amplifier provides a high dc gain at low frequencies. However, to ensure stability, the loop gain must decrease as frequency increases. The goal is to approximate a −20-dB/decade roll-off at all frequencies. Placing two zeros at the output filter's resonant frequency helps cancel the two poles representing the resonance. Adding a pole to the error-amplifier response cancels the zero that the output capacitor and its ESR introduce. Adding a final pole above the power supply's crossover frequency helps further increase the regulator loop's stability. **Figure 2b** shows the sum of the gains of the error amplifier and modulator/filter gain. The power supply's characteristics show a 30-kHz bandwidth and a 60° phase margin that ensures stable operation.

The power-supply-control-

(continued on pg 90)

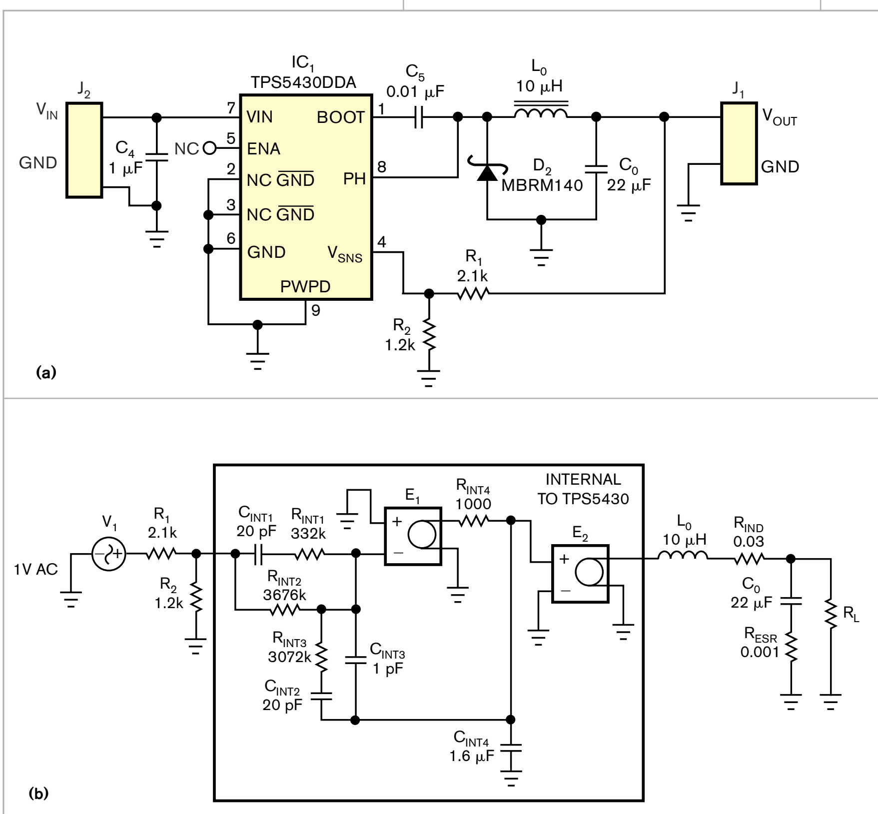


Figure 1 This TPS5430 power-supply design includes an aluminum electrolytic output-filter capacitor, C_0 (a). A circuit model includes parasitic resistances associated with output-filter components L_0 and C_0 (b).

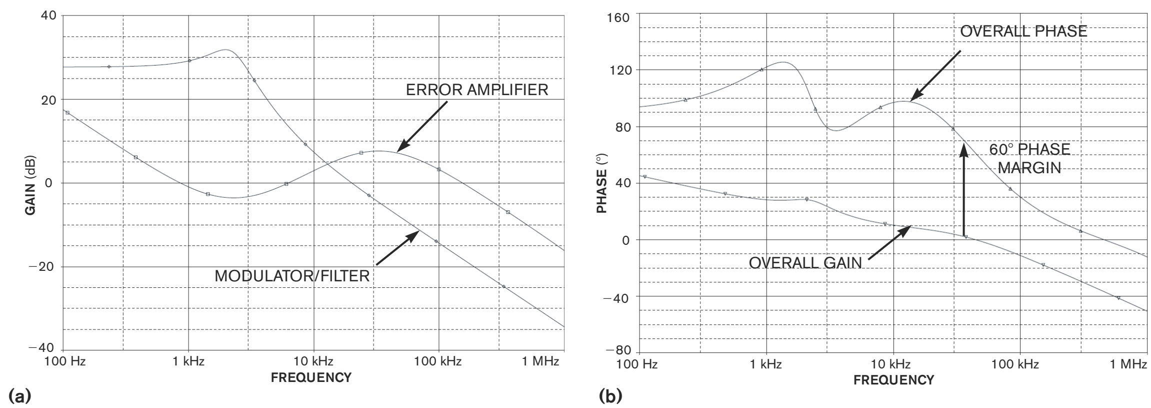


Figure 2 Gain (a) and phase (b) plots show that the circuit of Figure 1a includes adequate compensation and phase-angle margin for an aluminum electrolytic output-filter capacitor.

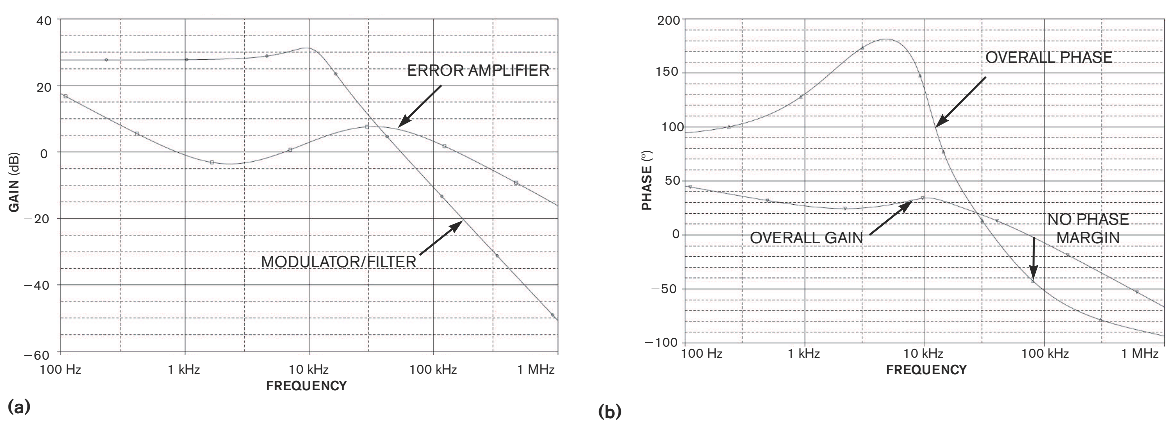


Figure 3 Gain (a) and phase (b) plots show that using a ceramic-dielectric output-filter capacitor erodes the phase-angle margin and pushes the circuit dangerously close to oscillation.

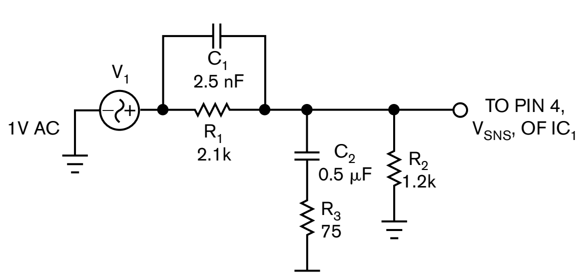


Figure 4 A few passive components supplement R_1 and R_2 and stabilize the circuit for use with a ceramic-dielectric output-filter capacitor.

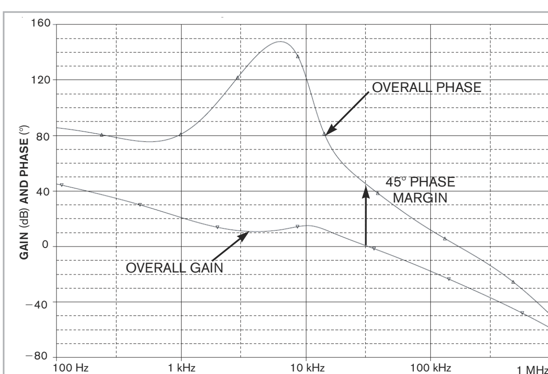


Figure 5 The phase-angle plot for the circuit of Figure 4 shows a sufficient phase-angle margin to allow stable operation with a ceramic output-filter capacitor.

loop response (**Figure 3**) illustrates the circuit's behavior when the design includes ceramic-dielectric output-filter capacitors and the same integrated-compensation components in **Figure 1**. Ceramic capacitors present a much lower ESR than do aluminum electrolytic capacitors, and their capacitance determines the filter's attenuation rather than their ESR. Consequently, at high frequencies, the LC filter's characteristics include a double pole and a steeper, −40-dB/decade slope. In addition, filter attenuation increases at the desired crossover frequency, degrading phase and gain margins. **Figure 3b** indicates that the power supply is unstable and, with no phase margin, will likely oscillate.

Replacing the divider network, R_1 and R_2 in **Figure 1** with the passive network in **Figure 4** stabilizes the regulation loop and allows an internally compensated controller to use ceramic output capacitors. The network's components add two sets of poles and zeros to the compensation network to cancel the consequences of using ceramic output capacitors. For example, C_2 and R_3 provide attenuation that reduces the crossover frequency. You select C_2 to provide attenuation at frequencies much lower than the crossover frequency. Unfortunately, C_2 adds a negative-phase shift that R_3 returns to nearly zero at the design's crossover frequency. Adding C_1 introduces a phase lead that compensates for the ceramic capacitors' negative effects. Without C_1, the filter's 180° phase shift would reduce the regulator's phase margin to nearly zero.

The phase angle starts increasing at a frequency that C_1 and R_1 determine, and they introduce a zero in the phase-plane plot at that frequency (**Figure 5**). At a frequency that C_1 and R_3 determine, a pole in the phase-plane plot terminates the phase angle's increase. The geometric mean of the pole and zero frequencies determines the maximum phase-angle boost.

As a starting point, you can place the first pole, which C_2 and the parallel combination of R_1 and R_2 determine, at a low frequency, such as 100 Hz. Next, adjust the values of C_2 and R_3 to set the first zero's frequency at 1 kHz, which is much less than the gain curve's 0-dB crossover frequency. Finally, set the zero that C_1 and R_1 introduce to a frequency that's at least a factor of two below the zero-gain crossover frequency to ensure a 45° phase margin at the crossover frequency. The Bode plot in **Figure 5** features a 30-kHz regulation-loop bandwidth that provides good transient response and more than 45° of phase margin to ensure good stability. EDN

REFERENCE

1 "Optimal Feedback Amplifier Design For Control Systems," Venable Industries, www.venable.biz/tp-03.pdf.

Tapped inductor, boost regulator deliver high voltage

David Ng and Adam Huff, Linear Technology Corp, Milpitas, CA

When you face the task of generating a regulated voltage that's higher than the available power-supply voltage, you may consider a boost regulator. Although a boost converter can in theory generate almost any voltage that's higher than its input, practical considerations limit the output to approximately eight times its applied voltage. To generate an even higher voltage, consider using a tapped-inductor boost topology. **Figure 1** shows an implementation of a converter that boosts a 3V input to 100V dc. The connections to the regulator chip are similar to those of a traditional boost converter, but, to achieve the high boost ratio, this design uses L_1, a 1-to-6-turns-ratio, tapped inductor.

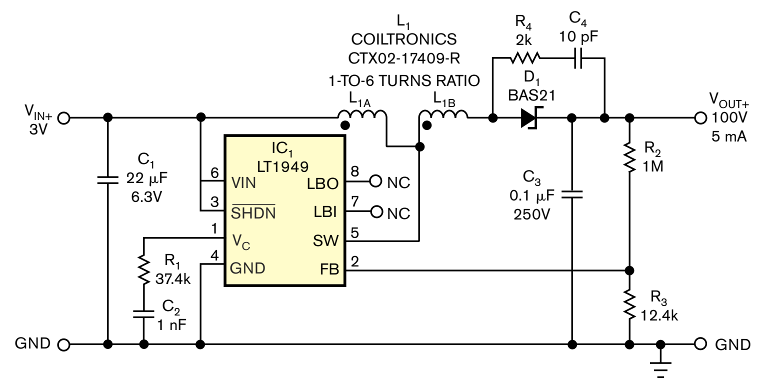


Figure 1 Using a tapped inductor extends a boost-topology switching regulator's practical output-voltage range.

The waveforms in **Figure 2** show the input voltage, the voltage at power-switch IC_1's output, Pin 5, and rectifier diode D_1's anode voltage. As in any boost circuit, inductor L_1's core stores energy when IC_1's internal output switch conducts. When the switch turns off, the voltage across its terminals and L_{1A} goes higher than the input voltage. Due to inductive coupling and the larger number of turns that make up L_{1B}, the voltage at rectifier diode D_1's anode and hence the output voltage goes much higher. Resistors R_2 and R_3 form a feedback-voltage divider that closes the regulation loop. The R_4-C_4 network forms a snubber circuit that suppresses the impact of diode D_1's small parasitic capacitance. Without the network,

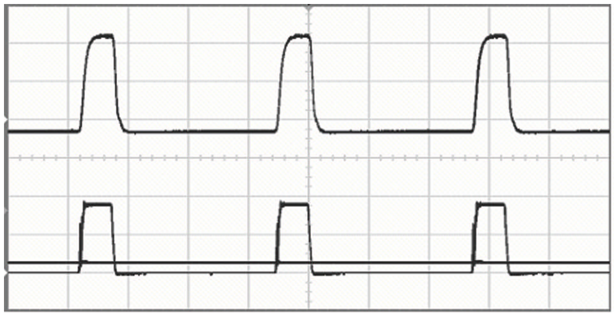


Figure 2 For a 3V-dc input (lower trace, horizontal line), the voltage at regulator IC_1's SW pin reaches a peak of approximately 18V (lower trace, pulsed waveform). The 1-to-6 step-up turns ratio of inductor L_1 further increases the peak output voltage to 160V (upper trace) to produce 100V dc. The upper trace's lower limit goes to $-6\times V_{IN}$ (−18V) due to the tapped inductor.

power switch IC_1 "sees" a capacitance that's 36 times larger due to the multiplicative effect of the tapped inductor's turns ratio.

Measuring only 5.6×6×3.4 mm, Coiltronics' (www.coiltronics.com) CTX02-17409 tapped inductor, L_1, and Linear Technology's (www.linear.com) LT1949 monolithic regulator, IC_1, available in an eight-lead MSOP package, present small pc-board footprints. When you implement the circuit on a single-layer pc board, the entire circuit occupies less than 1.9 cm^2 of board space (**Figure 3**). For best results, review the board-layout suggestions in the device's data sheet (**Reference 1**) and use multilayer-ceramic capacitors for C_1 and C_3. EDN

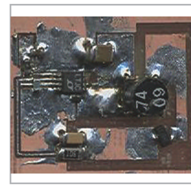


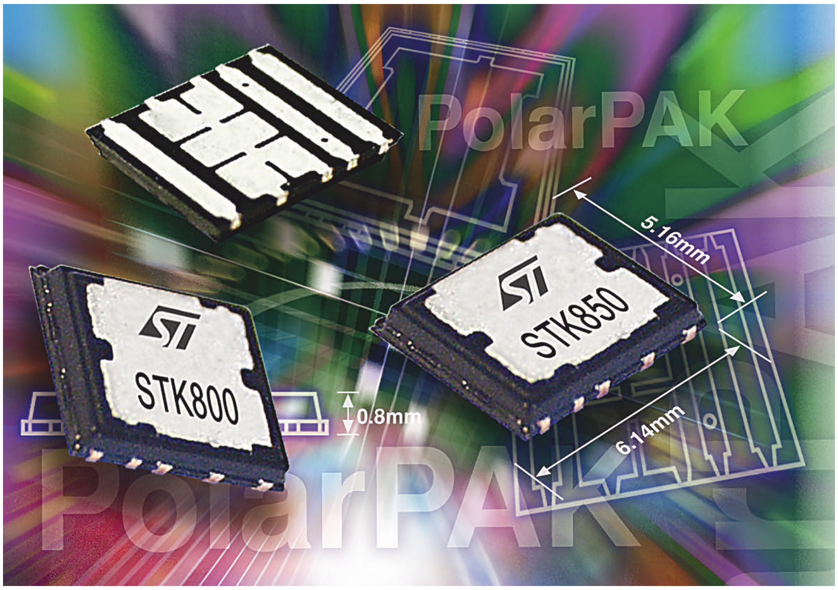
Figure 3 The entire boost-converter circuit occupies a footprint of less than 1.5×1.25 cm on a single-sided pc board.

REFERENCE

1. www.linear.com/pc/productDetail.do?navId=H0,C1,C1003,C1042,C1031,C1061,P1958.

productroundup

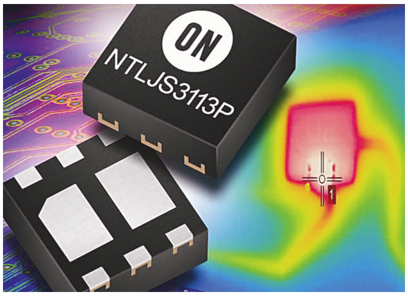
DISCRETE SEMICONDUCTORS



MOSFETs provide high thermal efficiency in compact package

Requiring the same 5×6-mm board area as an SO-8 package, the 20A STK800 and 30A STK850 power MOSFETs come in a PolarPak package, providing top and bottom heat-dissipation paths, resulting in a 0.8-mm profile. The lead-frame and plastic encapsulation are similar to those for standard power-MOSFET packages, ensuring good die protection and easy handling in manufacturing. Due to its increased heat dissipation, this device can handle twice as much current within the same footprint as standard SO-8 packages. The STK800 and STK850 cost $1.20 and $1.60 (1000), respectively.

STMicroelectronics, www.st.com



Power-MOSFET family has a small footprint

Aiming at portable-system applications, the new µCool family of power MOSFETs comes in a thermally enhanced, 2×2-mm WDFN6 package. These six products feature exposed-drain DFN technology, providing a 38°C/W thermal resistance and a 1.9W power rating. The devices have the same footprint dimensions as the SC-88 and SC-70-6 packages. The µCool family costs 29 to 31 cents (10,000).

On Semiconductor, www.onsemi.com

Ultrafast rectifiers maintain low power-supply losses

The 600V, 8A UH8JT and UHF8JT rectifiers provide a 25-nsec reverse-recovery time, decreasing switch-mode-power-supply losses. The devices combine improved switching performance with a 150-nsec forward-recovery time under test conditions and a 1.85V forward-voltage-drop rating at 125°C, improving thermal performance and system efficiency. The UH8JT and UHF8JT cost 35 cents each (10,000).

Vishay Intertechnology, www.vishay.com

GaN-transistor family targets cellular, WiMax-base-station markets

This family of GaN (gallium-nitride) HEMTs (high-electron-mobility transistors) targets cellular infrastructures and WiMax base stations. The devices feature a 67% peak drain efficiency at the UMTS (universal-mobile-telecommunications-system) frequency band and a 60% efficiency at the WiMax frequency band. The family's 8, 60, 90, and 120W devices aim at the UMTS or 3G-base-station segment. The 2.5-GHz transistors suit the WiMax-base-station segment and are available in 50, 75, and 100W options; 3.5-GHz, 8 and 50W options are also available.

RFMD, www.rfmd.com

Midvoltage MOSFETs target secondary-side synchronous rectification

The 60V IRF7855PbF, 80V IRF7854PbF, and 100V IRF7853PbF

productroundup

DISCRETE SEMICONDUCTORS

N-channel HEXFET MOSFETs come in a lead-free SO-8 package. These mid-voltage MOSFETs target ac/dc secondary-side synchronous rectification in 5 to 19V-output-voltage flyback-converter and resonant-half-bridge applications. These devices also suit isolated, medium-power dc/dc applications as primary-side switches in forward or push-pull topologies for 18 to 36V-input-voltage, isolated dc/dc converters. The IRF-7855PbF, IRF7854PbF, and IRF7853PbF cost $1.04, $1.06, $1.20, respectively.
International Rectifier, **www.irf.com**

Diodes feature a high temperature rating

The HVTD series diodes for down-hole, seismographic, automotive, and traction applications feature a 7000V rating and a 200°C temperature. These devices feature a 1-mA maximum forward current in oil, a 30-μA maximum reverse current, and an 18-μA typical reverse current. Devices in the HVDT series cost $4 (100).
HV Component Associates, **www.hvca.com**

TEST & MEASUREMENT

Measurement software builds and runs SCS applications

The latest version of DAPstudio measurement software allows users to design filters that roll off at 96 dB per quarter-octave and to build and run applications based on the vendor's SCS (signal-conditioning-system) series, requiring no additional data-acquisition software. Connecting directly to the sensors, the SCS also connects to specialized DAP boards, including iDSC 1816 boards, in PCs, providing additional channels of filtered 16-bit resolution data at $\pm$10 mV to $\pm$10V. The SCS/iDSC hardware costs $1000 per channel. The DAPstudio costs $199, and a free trial is available for downloading from the vendor's Web site.
Microstar Laboratories, **www.mstarlabs.com**

PCI Express analyzer aims at AMC form factor

Targeting the AMC (Advanced Mezzanine Card) form factor, the Vanguard Express PCI Express protocol and link analyzer can debug, test, and validate the PCI Express protocol and can test AMC.1 types 1, 2, 4, and 8 modules. Functioning as a self-contained unit, the analyzer installs between the device under test and the host system, allowing testing with minimal intrusion to the system under test. Features include independent and concurrent operation of both the analyzer and a statistics and protocol checker, a 256-Mbyte trace buffer, and eight trigger events. The Vanguard Express AMC costs $23,950.
VMetro, **www.vmetro.com**

Midrange DAP board uses an onboard Pentium processor

Operating from a 233-MHz Intel Pentium CPU, the midrange DAP (data-acquisition-processor) 5000a/526 board includes 16 analog inputs, two analog outputs, 16 digital inputs, and 16 digital outputs. External rack-mounted hardware allows for extending the channel counts to 512, 66, 128, and 1024, respectively. The device can acquire 14-bit data at 800k samples/sec and can convert 833,000 values/sec on the onboard analog outputs. An onboard processor allows fast real-time processing and a 0.1-msec task-time quantum latency. The DAP 500a/526 costs $3295.
Microstar Laboratories Inc, **www.mstarlabs.com**

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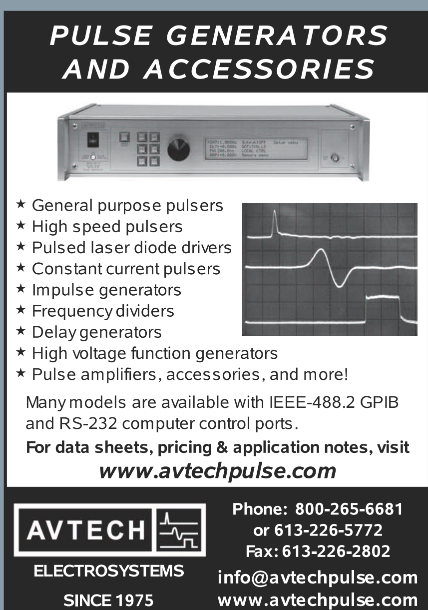

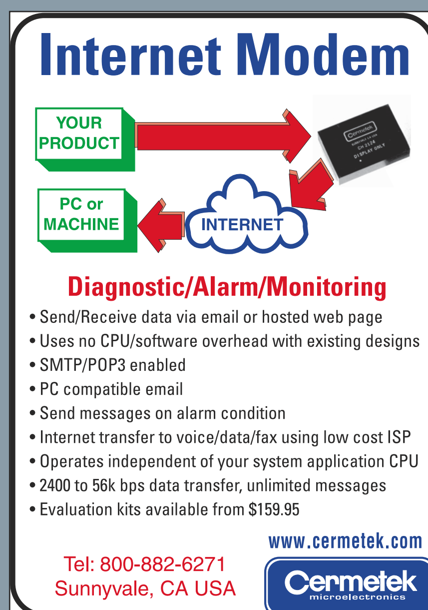

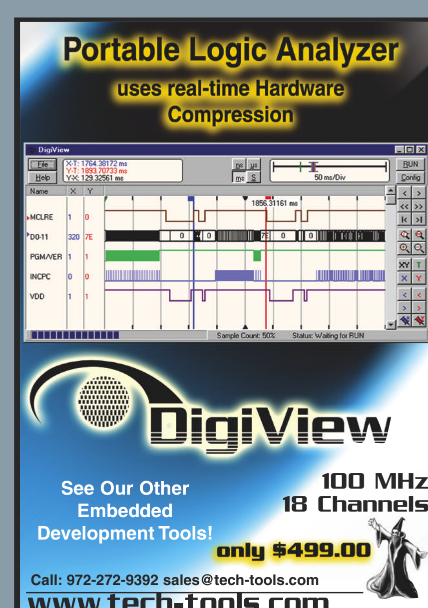

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realitycheck

YESTERDAY'S HYPE MEETS TODAY'S REALITY

STATS 30 hours between recharges / $1000 price tag / Offered handwriting recognition

Newton's life lesson

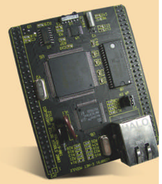
Apple Computer's Newton MessagePad PDA wasn't a big commercial success, but the complex product served a life lesson—to keep it simple—that Apple took to heart in its blockbuster iPod.

The Newton was to be Apple's next step in personal computing and portability beyond its Macintosh lineup. The system had a lot of leading-edge hardware and software to perform a large number of tasks. It combined word processing, a calendar, a calculator, an address book, and an infrared transceiver for wireless communications, among other features, as well as its main feature: handwriting recognition.

The system was one of the first major commercial devices to incorporate low-power ARM processors. The early units used an ARM6-based ARM 610, and later devices used a StrongARMSA-110. The Newton also used 4 Mbytes of flash and 4 Mbytes of DRAM. It offered 30 hours of runtime before needing a recharge—impressive for the mid-'90s. The device also incorporated a versatile OS that synchronized internally running applications with handwriting recognition.

Ultimately, the device failed to take off because it had trouble synchronizing with the outside world, it was too large to fit into a pocket, and it had a $1000 price tag. Ridicule of the handwriting-recognition feature in the *Doonesbury* comic strip didn't help, either.—by Michael Santarini

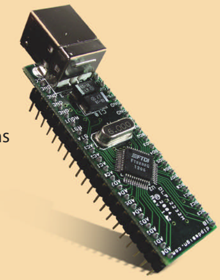
ZiLOG eZ80F915050MOD Development Module



The eZ80F91 operates at 50MHz with 256Kb on-chip Flash memory and 16Kb of internal SRAM, 512Kb of off-chip SRAM, 1Mb of Flash, and a 10/100BaseT Ethernet PHY with an RJ-45 connector. Oper. temp. 0°C to 70°C, 3.3V at 125mA, 2 x 60-pin system; MPU bus/control signals, IrDA transceiver.

ZiLOG mouser.com/zilog/a

DLP Design DLP-2232M Dual Channel USB Module



Uses FTDI's FT2232C 3rd generation dual channel USB-FIFO/UART; simple solution for interfacing ASIC/MCU/FPGA/DSP-based designs to host computer via USB; up to 8Mb per second, USB 1.1 compliant; no in-depth knowledge of USB required.

DLP Design mouser.com/dlpdesign/a

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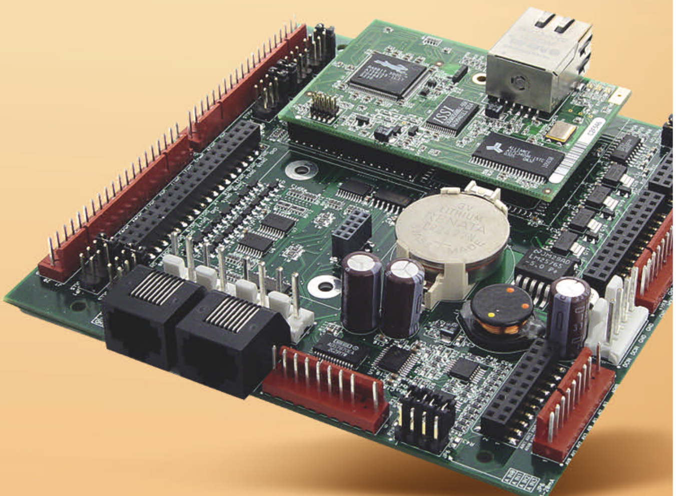

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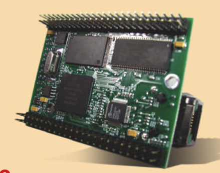
NetBurner MOD5272 32-bit Processor Module



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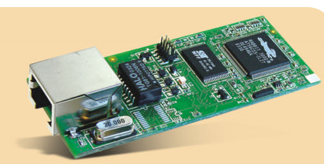
NetBurner Networking in 1 Day! mouser.com/netburner/a



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Features up to 512 Flash/ 512K SRAM, 4 serial ports, +5 VDC tolerant I/O, quadrature encoder inputs, PWM outputs, and a low-profile footprint (2.95" x 1.20" x .88").

RABBIT Semiconductor mouser.com/rabbitsemi/a

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Solutions

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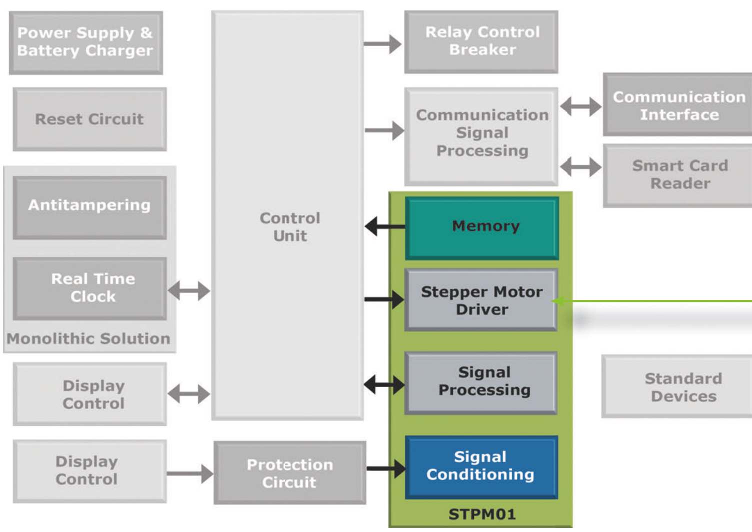

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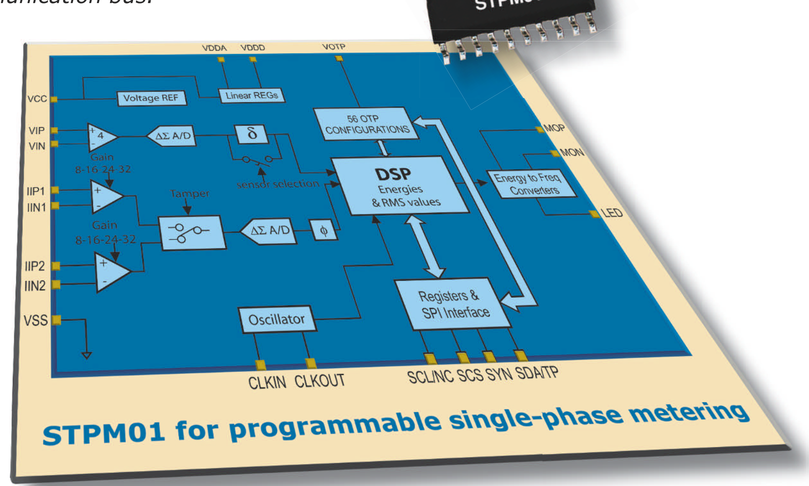

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- Ripple free active energy pulsed output
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- OTP for calibration and configuration
- Integrated linear VREGS for digital and analog supply
- Selectable RC or crystal oscillator
- Support 50÷60Hz, IEC 62052-11 and IEC 62053-2x specifications
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